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# Reduced Complexity MS Algorithm for Finding the First Two Minima in Tree Architectures

<sup>1</sup>S.SABARINATHAN, <sup>2</sup>K.DEEPADEVI

<sup>1</sup>Assistant Professor, <sup>2</sup>Post Graduate student, ME in Applied Electronics  
Department of ECE, Salem College of Engineering and Technology, Salem - 636 111.

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## ABSTRACT:-

**High speed architectures for finding the first two max/min values are of paramount importance in several applications, including iterative decoders and for proposed the adder and Low density parity check code (LDPC) has been implemented. The min-sum processing that it produces only two different output magnitude values irrespective of the number of incoming bit-to check messages. The new micro-architecture structures would employ the minimum number of comparators by exploiting the concept of survivor in the search. These result in reduced number of comparisons and consequently reduced energy use. Multipliers are complex units and play an important role in deciding the overall area, speed and power consumption of digital designs. The main feature of proposed algorithm is the use of the optimization factor. Also, the Optimization factor is not multiplied in posterior information which reduces complexity of the algorithm. By using the multiplier to reduce the parameters like latency, complexity and power consumption.**

## I. INTRODUCTION

In computer science a important role in many applications and a well established defect is sorting. In previous works it has been observed the sorting networks in hardware implementation are done very well. In communication field VLSI architectures and selection networks, are a part of various algorithms. For decoding

of turbo and binary Low-density- Parity-check(LDPC) codes, for maximum likelihood decoding of arithmetic codes in for k-best MIMO detectors, non-binary LDPC decoders also been used for non-binary LDPC decoders. When coming to systematic approach some works like gives a general problem of implementing parallel architectures for finding the first two max values.

A comparator based SM (Searching Module) is proposed by taking the concept form for sorting networks. As well as a radix sorting is used which is discussed, and form other approaches. A bitwise analysis data sorting is observed in radix sorting and prolongs to selection and partial sorting problems. An efficient sorting mechanism for finding first maximum/minimum values. The Explicit use of recursion in the constructions of error-correcting code is not new. In addition to the myriad constructions techniques shown in, many well-known codes involve construction of a long length codes from shorter codes.

For example, Elias' product code is straightforwardly recursive. The LDPC codes can also be seen to be recursive constructions when viewed as modifications of the basic product code construction and similarly Fowey's concatenated codes are another variations on the recursive theme of product codes, although there is no apparent advantage to more than one stage of recursions within framework. It is noteworthy that in all of these construction the conceptual simplicity of the recursions goes hand with simplicity in the computational process required for their implementation.

Although the threshold decoder for the codes can tend to hide the recursive structure, in all three of these techniques the conceptual decomposition of the recursion leads to a corresponding simplifying decomposition of the computational process. Unfortunately, all three would

like wise appear to testify that simplicity comes with a certain prices; the decomposition that affords the simplicity appears to prevents the long versions of the codes from being of the quality that is known to be possible, and the simple decoding algorithms are not even able to take advantage of the full power of the code.

While modifications to both the codes and the decoding algorithms can improve the situation, the improvements increase the complexity. Recursion has been a central concept in a closely related field of study: the design and analysis of computer algorithms and complexity theory. The complexity of a particular problem can often be understood by showing how the problems can be decomposed into smaller problems of the same type.

For example, an algorithm for sorting a large unordered lists of numbers consists of breaking the list into smaller list, sorting each of these, and then merging the small sorted list into successively larger sorted list. The analysis of the algorithm then focuses on the works required for the merging process, because it is the merge work needed for a given subdivision scheme that ultimately determine the growth of complexity. This same line of attack has proven fruitful in a wide variety of problems. In this to introduce a recursive approach to the construction of codes which generalizes the product code construction and suggests the design of algorithms for encoding and decoding is amenable to the basic techniques of complexity theory.

Long codes are built from bipartite graphs and one or more sub codes; a new code is defined explicitly by its decomposition into shorter sub codes. These sub codes are then used by the decoder as centers of local partial computations that, when performed iteratively, correct the errors. The decoding algorithms generalize and unify the decoding schemes originally presented the product codes and those of low density parity check codes. Correspondingly, the asymptotic growth rates are also comparable to that of these two low complexity schemes. Furthermore, the proper choice of the transmission order for the bits can guarantee good performance against burst errors or a mixture of burst and random errors.

## II. PROBLEM STATEMENT

1. The minima technique includes both main digital signal processor and error correction (EC) block.

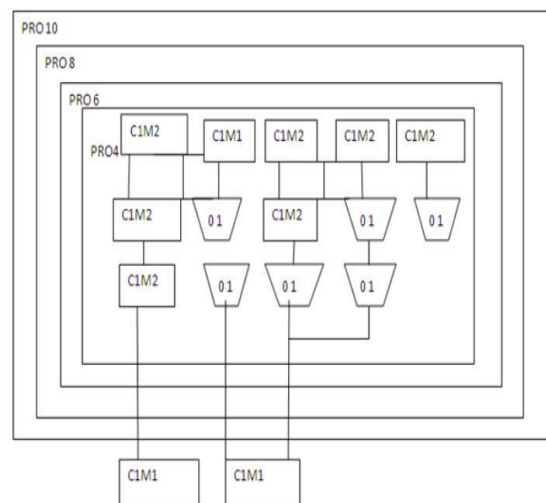
2. To meet ultralow power demand, minima and maxima is used in technique. However, under the complexity, once the critical path delay of the system becomes greater than the sampling period the soft errors will occur.

3. It leads to severe degradation in signal precision.

## III. PROPOSED EXPLANATION

In line with motivation and the previously explained normalized min-sum algorithm, to propose the optimized min-sum algorithm. The main feature of proposed algorithm is the use of the optimization factor. Multiplication of both in check nodes and bit nodes update is the basic difference between optimized min-sum algorithm and Normalized Min-sum algorithm. In this Normalized Min-sum algorithm, normalizing factor was used for check node update only. Also in 2 Dimensional Normalized Min Sum algorithm , two different factors for check and bit node updates are used and multiplied in 3 different places, check node processing. A posterior information and bit node processing.

The advantage of the proposed algorithm that only the optimization factor is used for both bit nodes and check nodes updates. Also, the Optimization factor is not multiplied in posterior information which reduces



complexity of the algorithm. The proposed algorithm is explained in where a flow chart is shown. First initialize the bit to check message. Then update the check

message in the horizontal step. The step, multiply the Optimization factor with the check message. After that, proceed to the vertical step. In this step, update the posteriori information with the help of check message and the update the bit node.

**Fig 1:** Tree based searching module for ten input

Here, multiply the Optimization factor with the check messages. The last step is the decision making process.

#### IV. TECHNIQUES:

##### Cyclic Redundancy Check

The CRC technique for detecting errors in digital data, but not for making corrections when errors are detected. It's used primarily in data transmission. In the CRC method, a certain number of check bits, often called a checksum, are appended to the messages being transmitted. The receiver can determine whether or not the check bits agreed with the data, to ascertain with a certain degrees of probability whether or not an error occurred in transmission.

If an error occurred, the receiver can send a "negative acknowledgement" back to the sender, requesting that the message be retransmitted. The CRC technique is also sometimes applied to data storage devices, such as a disk drive. In this situation each block on the disk have check bits, and hardware might automatically initiate a reread of the block when the error is detected and it might report the error to software.

The material that follows speaks in terms of sender and receiver of a "message," but it should be understood that it applies to storage writing and reading as well. The technique is based on polynomial arithmetic, in particular, on computing the remainder of dividing one polynomial in Galois field with two element by another. It is a little like treating the message as a very large binary numbers, and computing the remainder on dividing its by a fairly large prime such as Intuitively, one would expect this to give a reliable checksum.

##### Multiplexer

In electronics, a multiplexer device that selects one of several analog or digital input signals and forwards the selected inputs into a single line. A multiplexer of  $2^n$  inputs has  $n$  select lines, which are used to select which input line send to the output.

Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of times and the bandwidth a multiplexer is also called a data selector

Conversely, a demultiplexer device taking a single input signal and selecting one of many data-output-lines, which is connected to single input line. A multiplexer is often used with a complementary demultiplexer on the receiving end. An electronic multiplexer makes it possible for several signals to share one device or resource. An electronic multiplexer can be considered as multiple inputs and single output switch, and a demultiplexer as a single input and multiple output switch.

##### Digital Multiplexer

In digital circuits design, the selector wires are of digital values. In the case of a 2-to-1 multiplexer, a logic value of 0 would connect I2 to the output while a logic value of 1 would connect I1 to the output. In larger multiplexers, the number of selector pin is equal to  $\lceil \log_2(n) \rceil$  where  $n$  is the number of inputs. For example, 9 to 16 inputs would require no fewer than 4 selector pins and the 17 to 32 inputs would require no fewer than 5 selector pins. The binary value expressed on these selector pin determine the selected input pins.

A 2-to-1 multiplexer has a Boolean equations where A and B are the two inputs, S is the selector input, and Z is the output:

$$Z = (A \cdot \bar{S}) + (B \cdot S)$$

The different types of multiplexing technologies are given below

- Wavelength Division Multiplexer
- Frequency Division Multiplexer
- Dense Wavelength Division Multiplexer
- Reconfigurable Optical Add-Drop Multiplexer
- Orthogonal Frequency Division Multiplexer
- Add/Drop Multiplexer

### Decoding

To consider that the valid codeword, 101011, is transmitted across a binary erasure channel and received with the first and fourth bit erased to yield ? 01? 11. Since As with other codes, optimally decoding an LDPC code on the binary symmetric channel is an NP-complete problems, although techniques based on iterative belief propagation used in practice lead to good approximation. In contrast, belief propagation on the binary erasure channel is particularly simple where it consists of iterative constraint satisfaction.

The transmitted message must have satisfied the code constraints, the message can be represented by writing the received messages on the top of the factor graph. The example, the first bit cannot yet be recovered, because all of the constraint connected to it have more than one unknown bit. In order to proceed with decoding the message, constraint connecting to only one of the erased bits must be identified. In this either the second or third constraints suffices. Examining the second constraints, the fourth bit must have been 0, since only a 0 in that position would satisfy the constraints. This procedure is then it

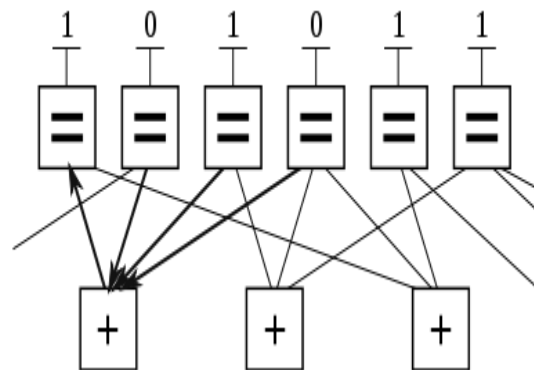


Fig 2 : Decoder

The new value for the fourth bit can be used in conjunction with the first constraint to recover the first bit as seen below. This means that the first bit must be 1 to satisfy the leftmost constraint.

Thus, the message can be decoded iteratively. For other channel models, the message passed between the variable nodes and check nodes are real numbers,

which express the probabilities and likelihoods of belief. This result can be validated by multiplying the corrected codeword  $\mathbf{r}$  by the parity-check matrix  $\mathbf{H}$ :

$$\mathbf{z} = \mathbf{H}\mathbf{r} = \begin{pmatrix} 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 \end{pmatrix} \begin{pmatrix} 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 1 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix}.$$

### V. CONCLUSION

A novel tree structure that finds the first two minima among many inputs and low complexity design is prominent requirement of iterative decoders. The complexity is reduced as the number of registers and memory consumption decreases. The overall synthesis result provides satisfactory performance for propagation delay i.e. the speed of the output is improved. VLSI implementation can be easily achieved with minimum consumption of area and power. Finally over all synthesis and testing can be implemented by using Xilinx. In tree structure, the candidates of the second minimum are collected by utilizing the results of comparisons performed for the first minimum. Hence, the proposed structure minimizes the number of comparators, leading to a low-complexity realization.

In addition, the second minimum is selected from the candidates by carrying out a few comparison steps. As the proposed structure eliminates the large-sized multiplexing networks, it improves the AT complexity significantly compared to those of the previous state-of-the-art SMs.

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