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6-bit, 180nm Digital to Analog Converter (DAC) Using Tanner EDA Tool for Low Power Applications

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Abstract

This paper describes a CMOS current-steering digital-to-analog converter with a full-swing output signal. In a Wireless system the quality of the communication link is main criteria, for great distance transmission it is necessary to convert analog signal into digital signal at input side, same as convert digital signal to analog signal at output side. In the Existing DAC, 6 Binary inputs to 63 thermometer-coded (unary) outputs will use 6-input NOR and NAND logic gate, and the timing delay of these gates are very different. As the clock rate rising, it will cause error decoding problems.so we propose the 6 to 63 thermometer decoder by 2 section decoding. There is two 3 to 7 thermometer decoder for column and row decoder. This scheme reduces the error decoding problems. A new scheme of the quaternary driver and an output current cell composed of both nMOS and pMOS.The nMOS operates from the power supply to the half of the supply. The pMOS operates independently from the half of the supply to the ground voltage. Then, the final output voltage is obtained through a multiplexer that is driven by a quaternary driver that selects the optimized current cell. The circuit is simulated using 180nm Complementary Metal-oxide Semiconductor technology at a power supply voltage of 3.0 V on Tanner tool and the power consumption is about 17.8 mW. The proposed Current Steering Digital to Analog converter are schematic using Tanner S-EDIT and simulation of the proposed work is done using Tanner T-EDIT. The waveform analysis is done using Tanner W-EDIT software

Index Terms: Binary to thermometer decoder, Current steering digital-to-analog converter (DAC), full-swing output, quaternary driver, TANNER EDA tool.

I. INTRODUCTION

Digital-To-Analog (D/A) converters are crucial components of modern applications such as video signal processing, digital signal synthesis, and both wired and wireless transmitters. Formerly, time-domain applications such as high-resolution performance and video signal processing were the main operator of high-speed D/A development. Accordingly, the emphasis was on specification parameters which were of importance for visual value: settling time, glitch performance, and linearity, especially integral nonlinearity (INL). The widespread use of digital modulation techniques has cause to more frequency-domain applications. For these applications, where the D/A converter (DAC) is used in the transmit path.The current system-on-a-chip (SOC) trends are toward integrating digital and analog circuits in a chip. As a result, a data converter, which is part of a vital interface within those systems, is becoming an increasingly more important block.[1]-[7] A digital-to-analog converter (DAC) is a representative circuit that a digital code is converted into an analog signal. Normally, the kinds of DAC are mainly divided into two categories: voltage-steering type and current-steering type. Since the settling time of the output voltage depends on the slew rate of the operational amplifier, voltage-steering type based on the op-amp for the DAC output is not suitable for high-speed applications. In the case of the current-steering type, the current generally flows directly through off-chip resistors or termination resistors inside the chip to obtain a fast operating speed. However, the output voltage at the termination resistor cannot have a full swing since the inevitable voltage drop is generated between the drain and the source of the output current cell.

In this brief, a current-steering DAC with a full-swing output voltage from the ground voltage to the power supply is proposed. The DAC has an architecture that follows the thermometer code method, which has excellent monotonicity and low glitch energy. The latch circuits have been simplified in order to reduce the power consumption and to correct mismatches.[2] In order to implement the full-swing output voltage, a quaternary driver and an output current cell composed of both nMOS and pMOS are discussed. First, the nMOS current cell operates from the power supply to the half of the power supply. Second, the pMOS current cell operates separately from the half of the power supply to the

ground voltage. Then, the final output voltage is acquired through a multiplexer that is driven by a digital driver that selects the optimized current cell. The contents of the brief are as follows. In Section II, the circuit design technique of the full-swing DAC is described. Measurement results and conclusions are summarized in Sections IV and V respectively.

II. DESIGN OF FULL-SWING CURRENT-STEERING DAC

The Current Steering consists of weighted currents produced by current mirrors, switches to steer the current and an added. The reference elements are current sources and sum elements are only wire connections. The switches are normally MOS transistors. The switches are controlled by the input bits. The every element is weighted with 21, 22, 23 ... 2N where N is the number of bits. The output current is given by

$$I_{out}=b_0 I_{unit}+b_1 2^{-1} I_{unit}+\ldots b_n 2^{-N} I_{unit}$$

The switches are controlled by the input word. Depending on the input word, the current source is switched to the load or to the ground which improves the speed of the DAC.

The advantage of current steering architecture is the ease of implementing the elements on the chip.

A. Architecture

Fig. 1 shows the block diagram of the full-swing DAC. The 6-bit digital input codes are arranged at the input data sync block to obtain the same delay time. The block 6-to-63 binary-to-thermometer decoder, the binary digital codes are converted into thermometer codes to improve the linearity and decrease the glitch noise. Then, the thermometer codes are transferred to the Giga latch, level shifter, and driver. Finally, the output currents are converted into analog voltages by the termination resistors. Generally, the 6-bit current-steering DAC is designed with a full matrix structure for high-speed operation and accuracy. Furthermore, there are many advantages such as a simple design, low integral nonlinearity and differential nonlinearity error, accurate monotonicity, low noise analog output, low glitches energy.

However, since the signals to drive the output current cell are entirely thermometer code, the complexity of the binary-to-thermometer decoder increases exponentially with DAC resolution.

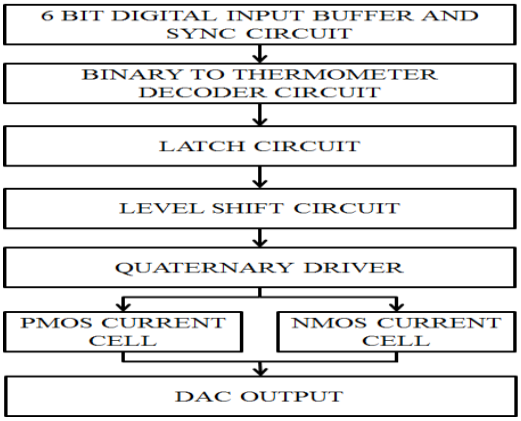

Fig-1: Block diagram of the full-swing DAC.

B. Digital Block

The output voltage cannot have a full swing. In order to solve this problem, it is necessary to add a level restoration circuit. The design example of thermometer decoder for the 4-bit binary digital input code. From 0000 to 0111, the output of the thermometer decoder is increased like a normal one. However, from 1000 to 1111, the output of the thermometer decoder is decreased like a reverse one. Thus, we can obtain 15 output codes at the thermometer decoder, and it operates like a symmetrical one. 6 to 63 binary to thermometer (unary) decoder consists of 6 input NOR and NAND gates and the timing delay of these gates are very different. As the clock rate rising, it will cause error decoding problems. After the end of the binary-to-thermometer decoder, the digital codes are holding at the Giga latch. Then, the digital signals of 1.8 V are shifted into 3.3 V at the level shifter. In order to have

the full-swing output analog signal at the current cell, a quaternary driver is proposed at the final digital block.

In the 6-bit DAC, there are 32 output current cells composed of both nMOS and pMOS. Since the current cells are driven by the proposed symmetrical thermometer decoder, we can obtain 63 codes at the output. With the thermometer decoder, the full-swing analog output voltage is obtained. It will be also discussed in the next section.

C. Analog Block

The output current cell is the most important circuit that dominantly determines the performance of the current-steering DAC. Thus, it needs a careful design to consider many factors. First of all, it must drive the correct current as one LSB and operate at a high speed. Furthermore, it must have a high output impedance to obtain good performances.

If the output impedance of the current cell is increased, it is possible to obtain the suitable current because it can minimize the swing of the current cell node. Those results improve not only INL and DNL, which are the static performance but also signal-to noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR), which are the dynamic performance. The Cell composed of four MOS: two MOSs are for switching MOSs and two MOSs are for the output current cell with CCM. In the case of the conventional current-steering DAC, the output voltage is determined by the operating range of the MOS. For example, if the nMOSs are only used, the output range is operated from the power supply voltage to weak GND. If the pMOSs are only used, the output range is operated from the weak VDD to the ground voltage. If we want to obtain the full swing output voltage, both pMOS and nMOS must be used. In order to improve the drawbacks of the conventional full swing current cell, a novel current cell with a digital driver is proposed. The digital driver is composed of four types that drive the output current cell, respectively. Thus, it is called the quaternary driver. Dependent on the digital code, the digital driver drives the appropriate digital value to the output current cell. The digital driver generates weak high positive, weak high negative, weak low positive, and weak low negative, respectively. This is because the switching MOS should be operated in the saturation mode, not in the linear mode. If the switching MOS is operated in the linear mode, there exists a voltage drop at the switching MOS. In order to minimize the voltage drop at the switching MOS, to reduce the error decoding problem and reduce glitch energy, therefore, the proposed digital driver is designed.

III. BINARY TO THERMOMETER DECODER

The Thermometer codes are the representation of numbers based on how many '1s' are present. The Binary to thermometer decoder is used to convert the N-bit binary input into 2N – 1 Thermometer coded output lines.

The decoder utilized for effective transformation of code from binary to thermometer for the realization of thermometric type digital to analog converter. The general idea of the decoder is based upon the detail that the decoder is the component which chooses one of the 2n outputs by decoding the binary value on the ‘n’ inputs. The binary to thermometer decoder is designed with the utilization of gates like AND, OR, NOT gate with CMOS 180nm technology.

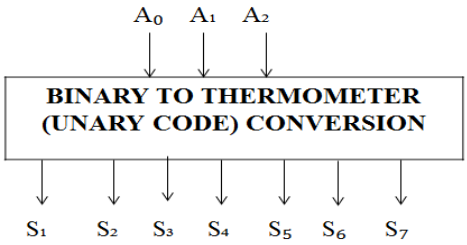

Fig-2: 3 to 7 block diagram Binary to Thermometer Decoder

In this execution, 6 bits are transformed into thermometer code. Thus we need 6 bit binary to thermometer decoder. To reduce the complexity, the 6-bit decoder is divided into two 3 bit decoders which are used for row and column of the unary current cell array. The 3 bit binary to 7-bit thermometer bit decoder is shown in fig. 2. Before sending the signals after first section decoding, we use the true single phase clock (TSPC) latch to convey the signals to the second decoding section (local decoder) in the case for high-speed data processing. It will reduce glitches energy.

IV. SIMULATION RESULTS OF PROPOSED DAC

The DAC is prepared in standard 180-nm CMOS technology. The power consumption is about 17.8mW with 1.2 V for the digital and 3.3 V for the analog. The fig. 3 shows the schematic diagram of Binary to Thermometer decoder. The 468 MOSFETs devices, 3 MOSFET geometries, 122 Subcircuit instances, 8 Boundary nodes, 235 Independent nodes, 243 Total nodes are present in the binary to thermometer decoder.

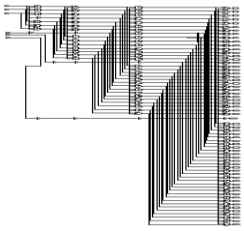

Fig-3: Schematic of Binary to Thermometer decoder

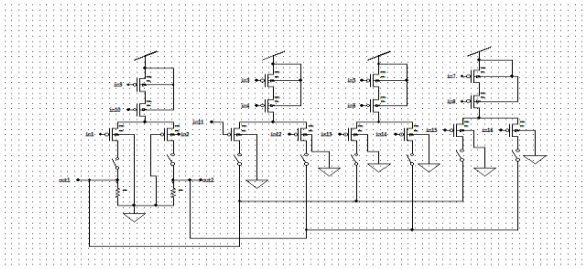

Fig.4: Schematic of PMOS current cell

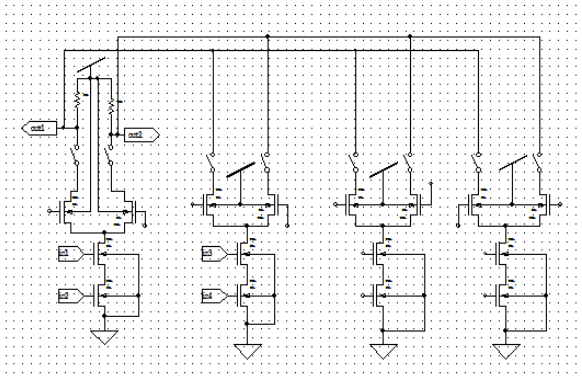

Fig.5: Schematic of NMOS current cell

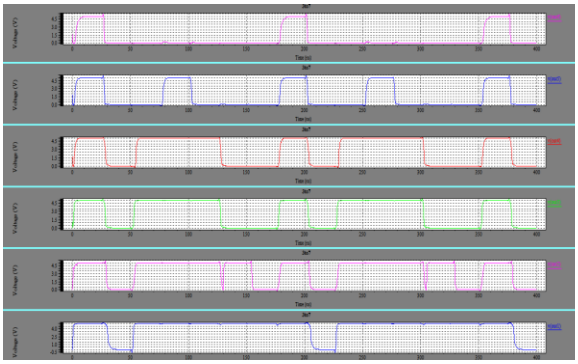

Fig.6: Waveform of Working of Binary to thermometer decoder

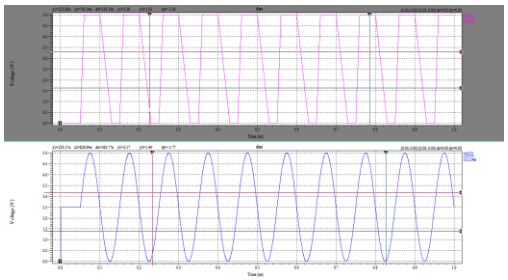

Fig.7: Waveform of Working of DAC

V. CONCLUSIONS

In this brief, a current-steering DAC with the full-swing output voltage was designed. The decoder was designed with two 3 to 7 binary to thermometer decoder for row and column. The current cell was composed of both pMOS and nMOS. Furthermore, the output voltage was driven by a quaternary driver that selects the optimized current cell. The power consumption was 17.8 mW. Table I shows the measured performance summary and the comparison with the conventional ones.

TABLE-1: PERFORMANCE SUMMARY AND COMPARISON

Parameters	[1]	[2]	[3]	This Work
Full Swing	YES [Buffer]	NO	NO	YES
Resolution	10-b	6-b	6-b	6-b
Technology	45nm	90 nm	0.13 µm	180nm
Power Consumption	476mW	8.32mW	29mW	17.8mW

VI. Future Work

However, the inconsistency between the pMOS current cell and the nMOS current cell is getting worse as the operating frequency is increased. Thus, it must be considered and solved in a near future. For example, an internal calibration circuit to guarantee the matching and consistency of the complementary current sources is absolutely needed in the real applications.

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