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A LOW POWER EFFICIENT DESIGN OF FULL ADDER USING TRANSMISSION GATES

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Abstract

A Full adder circuit is a very important component of the design of integrated circuits in VLSI design. In this paper represents a full adder using transmission gates at supply voltage is 1.8 dc voltages. The result of the post layout simulation (using CADENCE EDA TOOL) have been compare with the results of similar previously reported for adder circuits. In this proposed transmission gate circuits is very high efficient in terms of power, delay and area consumption compare too many other full adder circuits.

Key words: Pass Transistor Logic (PTL), Power-Delay Product (PDP), and Transmission gate (TG), Electronic Design Automation (EDA).

I.INTRODUCTION

Full adder is a fundamental unit of arithmetic operations. The important parameters of VLSI system in measuring performance based speed, coverage area & power consumption. High efficient circuits are desirable for any electronics gadgets. For supporting hardware should be equally inexpensive and compact. Arithmetic operations are useful in all the digital electronics system like digital image processing, image processing, video processing, arithmetic and logical units. Designing of low power and high speed full adder circuits with better performance. Here the full adders are designed with less supply voltages. Performance analysis is measured by taking different considerations like power consumption, total propagation delay and transistor count. In our work, a new transmission gates based 1 bit full adder has been proposed in its designing of improving performance.

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The next few paragraphs should contain the authors’ current affiliations, including current address and e-mail. For example, F. A. Author is with the National Institute of Standards and Technology, Boulder, CO 80305 USA (e-mail: author@ boulder.nist.gov).

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II.FULL ADDER BASICS

The full adder circuit have three inputs a, b & c and the outputs will be Sum and carry. Fig.1 shows basic block diagram of full adder.

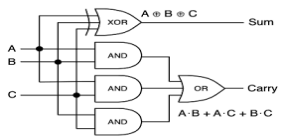

Fig.1 Full adder circuit

III.PREVIOUS WORK

The existing design of NMOS based low power 1 bit full adder has been designed using PTL technique. The existing adder has shown in fig.2

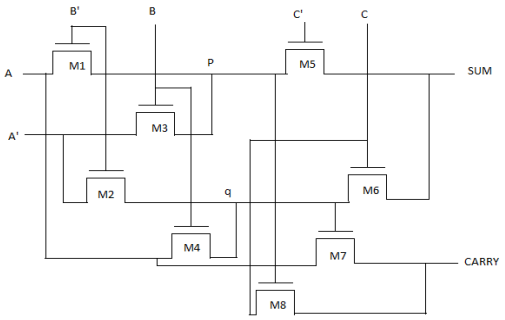

Fig.2 Existing 1 bit full adder

Sum = A ⊕ B ⊕ C

And Carry = AB + BC + CA

= AB + BC (A+A´) + CA (B+B´)
= AB + ABC + A´BC + AB´C
= AB (1+C) + (AB´ + A´B) C
= AB + (A ⊕ B) C

The first transistor M1 is generating output AB´ while M3 is generating A´B. The two outputs together generate (A ⊕ B) at point p. Outputs of M2 and M4 are A´B´ and AB respectively. It produce (A B) after meeting at point q. The logic at the outputs of M5 and M6 are (A ⊕ B) C´ and (A B) C. So the Sum output is

Sum = (A ⊕ B) C´ + (A ⊕ B)´ C = A ⊕ B ⊕C

Similarly, the output logics of M7 and M8, (A B) A and (A ⊕ B) C, together generate Carry output as:

Carry = (A B) A + (A ⊕ B) C
= (AB + A´B´) A + (A ⊕ B) C
= AB + (A ⊕ B) C

The logic values at the output levels are listed in Table 1:

Table1. Truth table of existing full adde

A	B	C	M1	M2	M3	M4	M5	M6	M7	M8	Sum	Carry
0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	1	0	0	1	0
0	1	0	0	0	1	0	1	0	0	0	1	0
0	1	1	0	0	1	0	0	0	0	1	0	1
1	0	0	1	0	0	0	1	0	0	0	1	0
1	0	1	1	0	0	0	0	0	0	1	0	1
1	1	0	0	0	0	1	0	0	1	0	0	1
1	1	1	0	0	0	1	0	1	1	0	1	1

IV.PROPOSED WORK

A transmission gate is both PMOS and NMOS parallel with each other. It is similar to a relay that can conduct in both directions. It is CMOS based switch in which PMOS passes a strong 1 but poor 0 and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work together simultaneously.

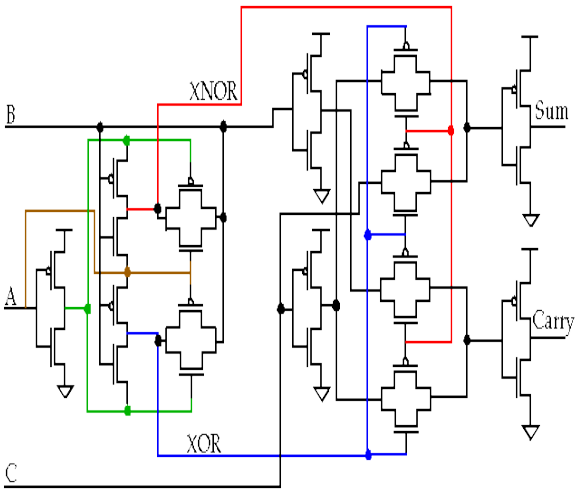

Fig.3 The Proposed adder circuit

The Proposed design is transmission gates of low power 1 bit full adder shown in fig.3

V.SIMULATION RESULTS

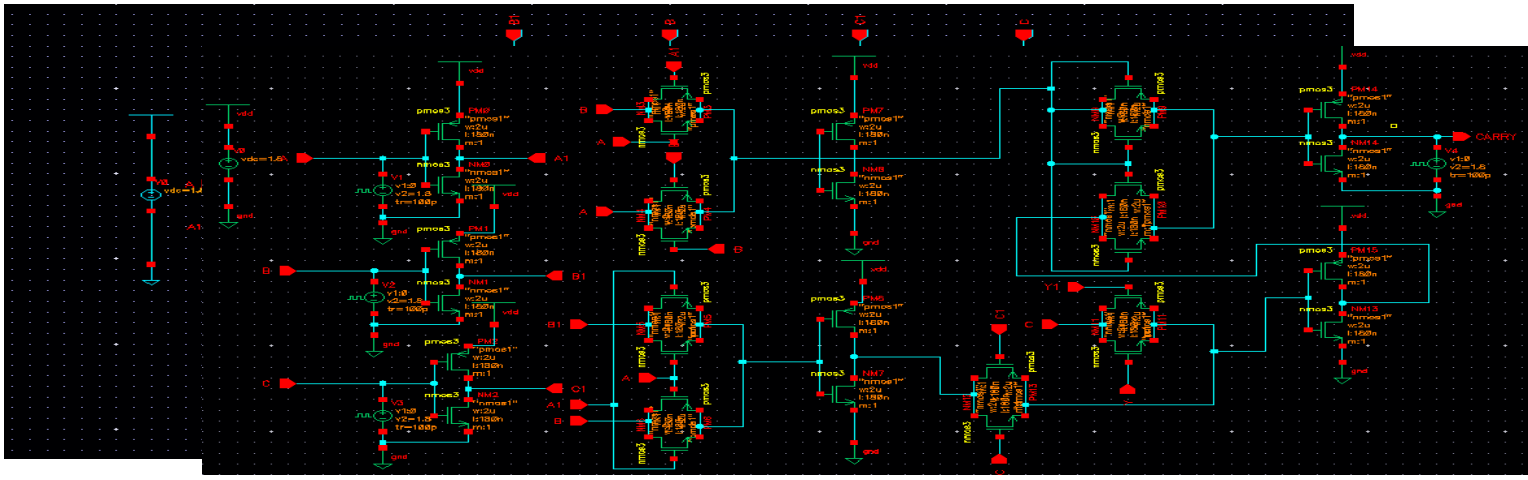

Fig.4 Schematic Of Existing Design

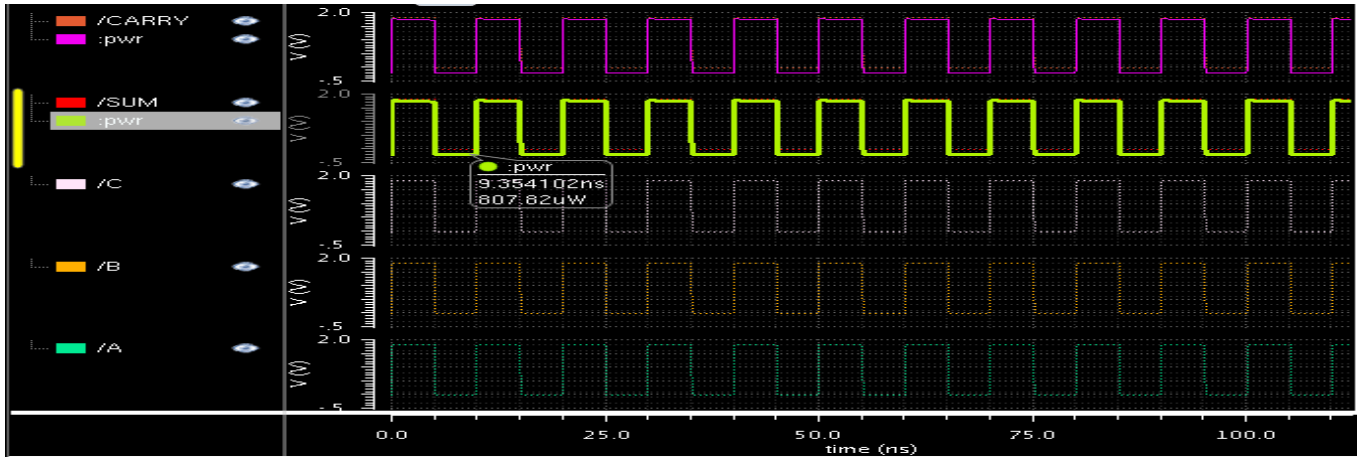

Fig.5 Output of Existing Design

Fig.5 Schematic Of Proposed Design

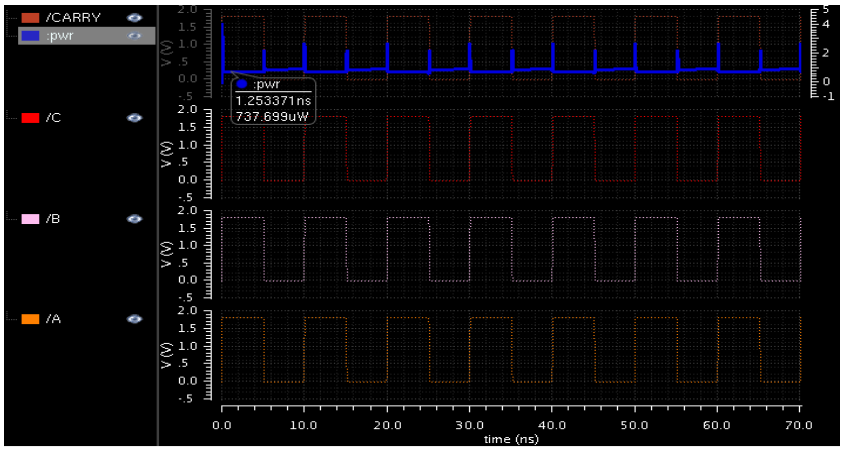

Fig.5 Schematic Of Proposed Design

VI.RESULTS COMPARISON

Table 2. Results comparison

Design	Power	Delay	PDP
N-MOS based full adder	807.82uW	9.354102 ns	7.5664 PJ
Transmission Gates using full adder	737.69uW	1.25337 ns	0.9245 PJ

VI.CONCLUSION

In this paper, the proposed design of transmission gates using 1 bit full adder is very useful technique to reduce power and chip area. So we conclude the transmission gate design analysis is to find better results compare to previous design of full adders. The Performance degradation and the internal load capacitance of this circuit are much less compared to previous design. So the proposed full adder circuit provides better power delay product compared to NMOS based 1 bit full adder.

REFERENCES