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MULTI LEVEL ELECTRONIC BANK LOCKER SECURITY SYSTEM

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Abstract

In this developing world, safety and security is given the prime importance. In the day-to-day life there come various situations in which security is being challenged. Lots of money is being sent and extensive researches are going on for developing reliable security access control systems. The need for developing an error free and cheap security system is greatly demanding. It will be a boon in many sectors like banking, defense and finance. We here try to give a report on a security system. The following abstract gives an idea about a reliable security system with the help of which, the above-discussed problem can be overcome to a little extent. Absence of reliable security systems can lead to great chaos or a catastrophe. In keypad system a password or a Personal Identification Number (PIN) is set in the microcontroller. The password may have numbers or characters. By typing that particular password one can get access to system.

This project "MULTI LEVEL ELECTRONIC BANK LOCKER SECURITY SYSTEM" is a reasonable solution in terms of security and access control. This system has a software running in PC from which manager can enable the bank lockers. After enabling, the individual lockers can be accessed by the users . In this system any number of users can login or logout simultaneously by getting access from the manager. Thus the system seemed to be more secured & advanced than any other current technologies. It can be also used in any fields where high SECURITY CONTROLS are required.

Introduction

We are now living in the world of machines. Everything in the world is controlled by electronics, which has made this world fast and sophisticated. Security is becoming a major factor in this present scenario. Security is a big challenge in sectors such as defense, banking, finance and power plants. Absence of reliable security systems can lead to great chaos or a catastrophe. This project "**MULTILEVEL ELECTRONIC BANK LOCKER SECURITY SYSTEM**" is a reasonable solution in terms of security and access control.

Security of the valuables is the main concern of every household and business entity. The concern increases by manifolds in the arena of banking and jewelry trade.

Bank safe deposit lockers include several deposit cabinets with cells specially designed to secure valuables (protected by two key and electronic-mechanical access and security system).

DESIGN PROCEDURE

Overall Schematic Design

To create the overall schematic of design, first individual schematics of different modules of the design were gathered. The components forming the modules were already short-listed and purchased, their selection depending on their features and availability. The integrated circuit companying each module of the design was obtained from the individual schematics available from the manufacturers. Especially in the case of power supply circuits, there were many proven example circuits available, the most suitable option being chosen.

The main challenge of the overall schematic design was putting these different modules together. After hours of studying the flow of information from each module to another and with the help of the faculty at KELTRON, the final schematic was obtained. The overall schematic includes the interface between the modules. The board schematics are included in Appendix A. As well as these modules, the schematic also includes the components that make it more convenient for the user to obtain information from the

design. It includes pinheads that could be used for the user to implement further functionalities and modifications.

The main component of the circuit is the Atmel 89C52 microcontroller which receives the data from the key board. The crystal oscillator generates the clock pulse by which all internal operations are synchronized. An LCD display connected to the microcontroller via a display driver displays the data being transmitted for verification purposes. There is a power supply circuitry supplying power at the required voltage to the various ICs.

Board Design

After creating the overall schematic of the design, the next step was to create a board that is simple, compact, and easy to use and install. ORCAD Capture CIS 9.2 was the PCB Design software used to create such a board. We found Capture very convenient to use in designing the board because of its user-friendly interface and extensive libraries. Using Capture, the schematic diagrams for the transmitter, receiver and serial communication modules were drawn. The schematic diagrams can be seen in Appendix A. The PCB layout of the transmitter module on the consumer side unit and receiver module on the authority side unit were obtained thus from the schematic diagram. PCB layout is included in Appendix B. The serial communication module, being relatively simple was fabricated on a multi-purpose board.

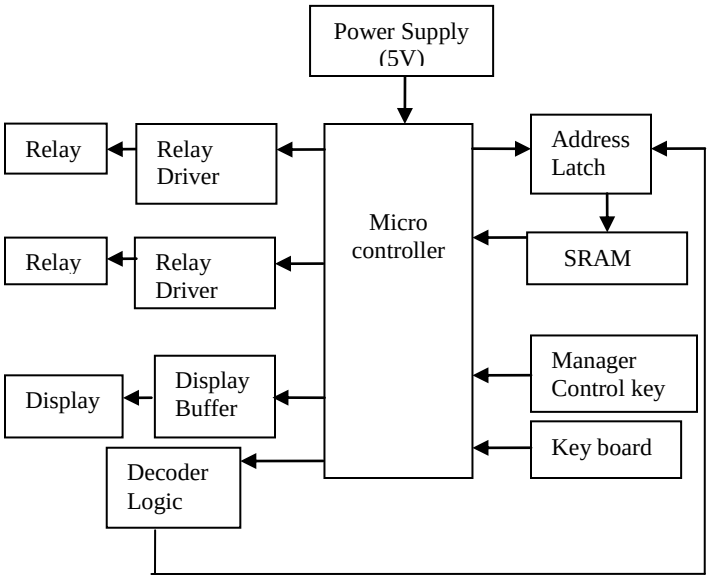
Programming

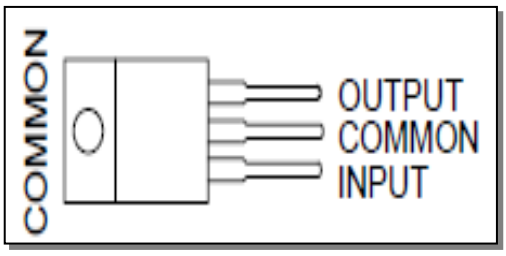
8. 3. a. Assembly Language Programming

The programming for the AT89c52 microcontrollers on the transmitter and receiver modules was developed next. With a rudimentary knowledge of 8085 assembly programming in hand, we conducted a study of the AT89c52 instruction set. An algorithm was designed for the required functionality of the microcontroller. Based on it, assembly language program for the microcontrollers on the transmitter and receiver boards were written. We were suitably guided on this endeavour by the staff at KELTRON.

In the transmitter board, the microcontroller is programmed to count the pulses, control the LCD display and send the data to the transmitter. In the receiver board, the microcontroller receives the data and passes it on to the serial communication module. The developed assembly language code is included in Appendix C.

BLOCK DIAGRAM





BLOCK DIAGRAM DESCRIPTION

The main unit of the circuit is the 89C52 micro controller. The crystal oscillator circuitries generate the clock pulse by which all internal operations are synchronized. The reset pin of 89C52 is

active high. In order to activate this whenever necessary a reset circuitry is provided. The crystal oscillator has a frequency of 11.059MHZ. this particular frequency of the crystal oscillator is used to make serial communication easy for further development of the project. Address latch (74ls373) is used to demultiplex the low order address/data lines from the microcontroller. IC 62C256 , 32K SRAM is used as the memory in this circuit. Another ic 74ls373 is used as the display buffer which is connected to the LCD display. Decoder logic (74ls138 & 74ls20) is used for address decoding in this circuit. +12V power supply is required for the relays. +5V is needed as VCC for all the ICs used in this circuit. An electronic energy meter is used in this circuit to calculate the power

IMPORTANT COMPONENTS
MICROCONTROLLER UNIT-AT89C52
POWER SUPPLY UNIT-+5 V and +12 V
ADDRESS LATCH-74LS373
32 K SRAM- IC 62C256
DECODER IC's- 74ls138 and 74ls120

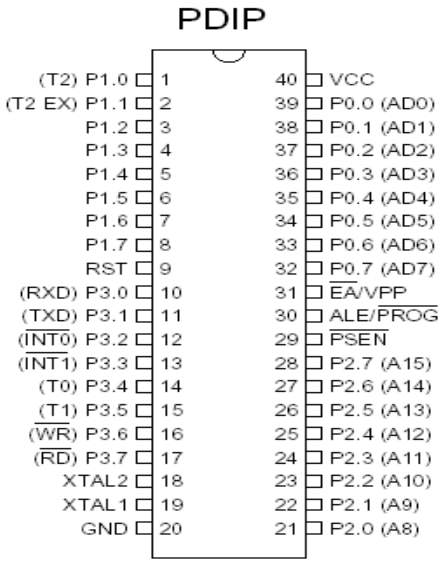
LM7805: Voltage Regulator
LM7805 and LM 7812 are positive voltage regulators that can deliver up to 1.5 A of output current. The internal current-limiting and thermal-shutdown features of these regulators essentially make them immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents, and also can be used as the power-pass element in precision regulators.

MICROCONTROLLER 89C52

The AT89C52 is a low-power, high-performance CMOS 8-bit microcomputer with 8Kbytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 and 80C52 instruction set and pinout.

The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C52 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

Features
• Compatible with MCS-51™ Products
• 8K Bytes of In-System Reprogrammable Flash Memory
• Endurance: 1,000 Write/Erase Cycles
• Fully Static Operation: 0 Hz to 24 MHz
• Three-level Program Memory Lock
• 256 x 8-bit Internal RAM
• 32 Programmable I/O Lines
• Three 16-bit Timer/Counters
• Eight Interrupt Sources
• Programmable Serial Channel
• Low-power Idle and Power-down Modes.
6.1.2 BLOCK DIAGRAM
Pin Configuration



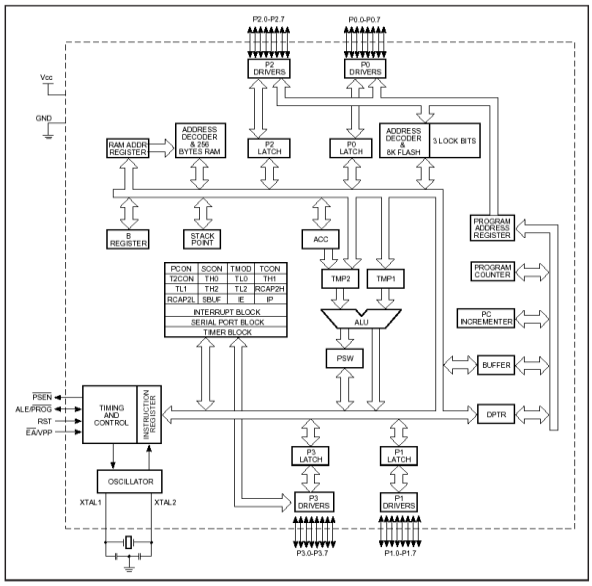


Figure 4. IC89C52(51)A Block Diagram

The AT89C52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full-duplex serial port, on-chip oscillator, and clock circuitry. In
addition, the AT89C52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next hardware reset.

PIN DESCRIPTION

VCC
Supply voltage +5v DC
GND
Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs. Port 0 can also be configured to be the multiplexed low order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull ups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull ups. In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the Timer /counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table. Port 1 also receives the low-order address bytes during flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the

high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pull-ups. Port 3 also serves the functions of various special features of the AT89C51, as shown in the following table. Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN

Program Store Enable is the read strobe to external program memory. When the AT89C52 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions.

This pin also receives the 12-volt programming enable voltage
(VPP) during Flash programming when 12-volt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

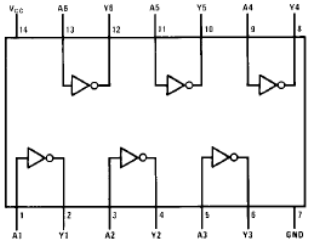
Output from the inverting oscillator amplifier

DM 74LS14

Hex Inverter with Schmitt Trigger Inputs General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteretic which increases the noise immunity and transforms as lowly changing input signal to a fast changing, jitter free output.

Connection Diagram



Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

HM 62256: CMOS Static RAM

The KM62256C family is fabricated by Samsung's advanced CMOS process technology. The family supports various operating temperature ranges and has various package types for user Flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

General Description Features

i. Process Technology : 0.7□m CMOS
ii. Organization : 32Kx8
iii. Power Supply Voltage : Single 5V□10%
iv. Low Data Retention Voltage : 2V(Min)
v. Package Type: 28-DIP-600, 28-SOP-450, 28-TSOP1-0813.4F/R
vi. Three state output and TTL Compatible.

74F138

1-of-8 Decoder/Demultiplexer

General Description

The F138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three F138 devices or a 1-of-32 decoder using four F138 devices and one inverter.

Features

- ❖ Demultiplexing capability
- ❖ Multiple input enable for easy expansion.
- ❖ Active LOW mutually exclusive outputs.

Functional Description

The F138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs (O_0–O_7). The F138 features three enable

Inputs, two active LOW (E_1, E_2) and one active HIGH (E_3). All outputs will be HIGH unless E_1 and E_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four F138 devices and one inverter (See Figure 1). The F138 can be used as an 8-output duplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied.

MM74HC373

3-STATE Octal D-Type Latch

General Description

The MM74HC373 high speed octal D-type latches utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system. When the LATCH ENABLE input is HIGH, the Q outputs will follow the D inputs.

When the LATCH ENABLE goes LOW, data at the D inputs will be retained at the outputs until LATCH ENABLE returns HIGH again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to VCC and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 □A maximum
- Low quiescent current: 80 □A maximum (74 Series)
- Output drive capability: 15 LS-TTL loads.

DM74LS08

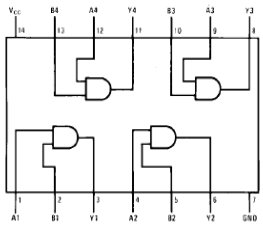
Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which Performs the logic AND function.

74ls06

Connection Diagram



Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

Convert TTL Voltage Levels to MOS Levels

_ High Sink-Current Capability

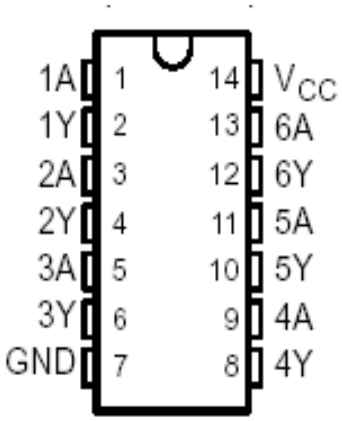
_ Input Clamping Diodes Simplify System Design

_ Open-Collector Driver for Indicator Lamps and Relays

_ Inputs Fully Compatible With Most TTL Circuits.

Description/ordering information

These hex inverter buffers/drivers feature high-voltage open-collector outputs to interface with high-level circuits (such as MOS), or for driving high-current loads, and also are characterized for use as inverter buffers for driving TTL inputs. The 'LS06 devices have a rated output voltage of 30 V, and the SN74LS16 has a rated output voltage of 15 V. The maximum sink current for the SN54LS06 is 30 mA, and for the SN74LS06 and SN74LS16 it is 40 mA.



HM 62256

32Kx8 bit Low Power CMOS Static RAM

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- Organization : 32Kx8
- □Power Supply Voltage : Single 5V□10%
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- Three state output and TTL Compatible
- Package Type : 28-DIP-600, 28-SOP-450, 28-TSOP1 -0813.4F/R.

CONCLUSION

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2. LOCKER SECURITY SYSTEM USING RFID AND GSM TECHNOLOGY Aruna.D.Mane1 and Sirkazi Mohd Arif2 1M. Tech (Digital Electronics), Department of ECE, SIET, Bijapur, Karnataka, India 2B.E (ECE), Department of ECE, SIET, Bijapur, Karnataka, India from International Journal of Advances in Engineering & Technology, May 2013. ©IJAET ISSN: 2231-1963.