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Fixed Width Booth Multiplier Using Adaptive Conditional Probability Estimator

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ABSTRACT

Adaptive Conditional Probability Estimator technique is applied to fixed width booth multiplier .It is applied based on the theory called Conditional-Probability theory. The ACPE can be easily applied to more than 16bit Booth multipliers for achieving a higher accuracy performance. The ACPE provides varying column information to adjust the accuracy with respect to system requirements. The area and power can be reduced to considerable amount compared with the existing methods.

Hardware complexity is reduced and power saving can also be achieved. The truncation errors have been hugely reduced. This ACPE Booth multipliers can also be applied to the two-dimensional cosine transforms to demonstrate the performance of real time applications.

Index Terms – Adaptive conditional Probability estimator (ACPE),Booth Multiplier, Discrete cosine transform(DCT),fixed-width.

INTRODUCTION

High processing performance and low power dissipation are the most important objectives in many multimedia and digital signal processing systems, where multipliers are always the fundamental arithmetic unit and significantly influence the system's performance and power dissipation. To achieve high performance, the modified Booth encoding which reduces the number of partial products by a factor of two through performing the multiplier recoding has been widely adopted in parallel multipliers.these lossy systems which allow a little accuracy loss to output data.

The fixed-width Booth multiplier with the best accuracy is the post truncated (P-T) multiplier, which uses rounding off operator after calculating all products. However, the P-T multiplier consumes large silicon area in Very Large Scale Integration (VLSI) designs. In order to reduce the area cost, the Direct-Truncated (D-T) multiplier chops the least significant half partial products directly. Thus, a large number of truncation errors occur in the D-T Booth multiplier. For this reason, the adaptive compensation methods for fixed-width Booth multipliers are presented to reduce the truncation errors while still reserving the merits of low area cost.A low cost compensation bias is approximated from a linear regression. The errors can be reduced hugely compared with the D-T Booth multiplier.

Booth's Multiplication algorithm:

Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation.Booth's algorithm can be implemented by repeatedly adding (with ordinary unsigned binary addition) one of two predetermined values *A* and *S* to a product *P*, then performing a rightward arithmetic shift on *P*.

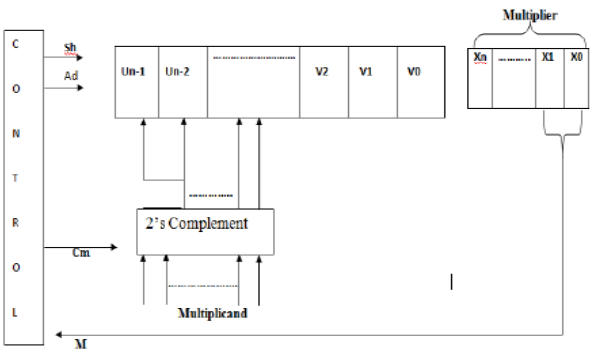


Fig: Block diagram of Booth's multiplier

Working Operation

Consider a positive multiplier consisting of a block of 1s surrounded by 0s. For example, 00111110. The product is given by

$$M \times 00111110 = M \times (2^5 + 2^4 + 2^3 + 2^2 + 2^1) = M \times 62 \quad (3.4)$$

where M is the multiplicand.

The number of operations can be reduced to two by rewriting the same as

$$M \times 010000 - 10'' = M \times (2^6 - 2^1) = M \times 62 \quad (3.5)$$

In fact, it can be shown that any seque nce of 1's in a binary number can be broken into the difference of two binary numbers. This scheme can be extended to any number of blocks of 1s in a multiplier (including the case of single 1 in a block).

Thus,

$$M \times 00111110 = M \times (2^5 + 2^4 + 2^3 + 2^2 + 2^1) = M \times 58 \quad (3.6)$$

$$M \times 010000 - 10'' = M \times (2^6 - 2^3 + 2^2 - 2^1) = M \times 58$$

(3.7)

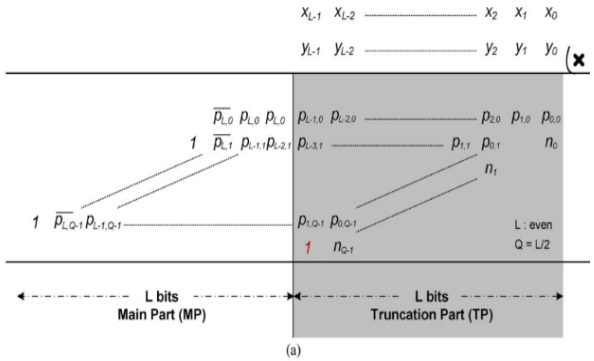
PROPOSED METHOD

A high-accuracy Adaptive Conditional-Probability Estimator is to be applied in fixed-width Booth multipliers., the ACPE is derived from the conditional-probability theory. Thus, the ACPE can be easily applied to large length Booth multipliers.

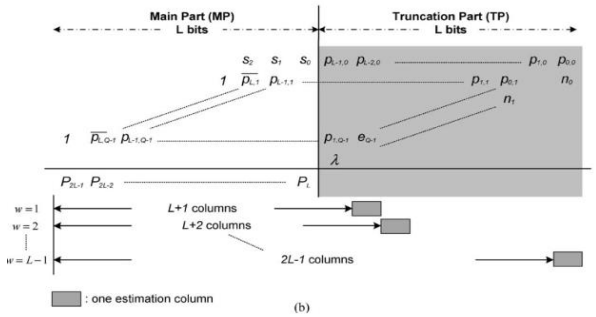
Fixed width multipliers are the important components in digital signal processing systems. In general, they truncate the least significant half part directly to generate the output with the same word length as input, and the computation errors occur from the operators that perform the truncation. eleThe fixed-width Booth multiplier with the best accuracy is the post-truncated multiplier, which uses rounding off operator after calculating all products. However, the P-T multiplier consumes large silicon area in very large scale integration designs. In order to reduce the area cost, the direct-truncated multiplier chops the least significant half partial products directly. Thus a large number of truncation errors occur in the D-T Booth multiplier.

Fixed width Modified Booth Multiplier

The main part including the most significant columns, and the truncation part including the least significant column. The column information is included to adjust accuracy with respect to system requirements.



(a) Conventional P-T Booth algorithm of L×L Booth multiplier.



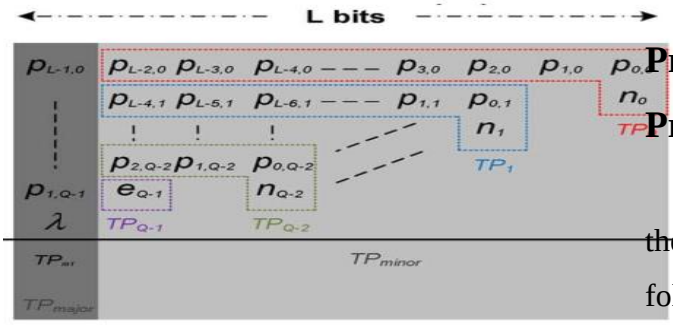
(b) Modified algorithm of L×L Booth multiplier.

Fig. 4.2.1 Algorithms of L×L fixed-width Booth multipliers.

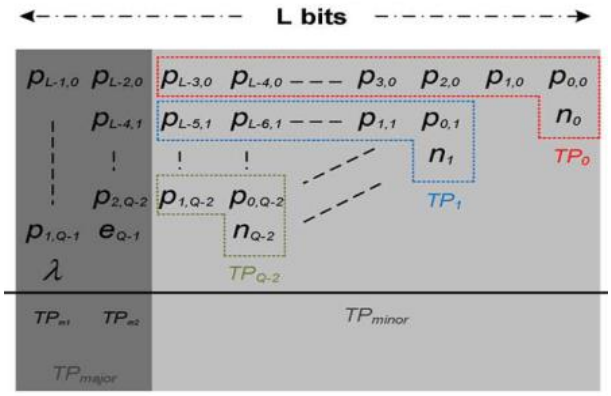
Table 4.2.3: Mapping table of modified booth algorithm

n_{Q-1}	$P_{0,Q-1}$	$P_{L,0}$	S_2	S_1	S_0	λ	e_{Q-1}
0	0	0	1	0	0	1	0
0	0	1	0	1	1	1	0
0	1	0	1	0	0	1	1
0	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1
1	0	1	0	1	1	1	1
1	1	0	1	0	1	0	0
1	1	1	1	0	0	0	0

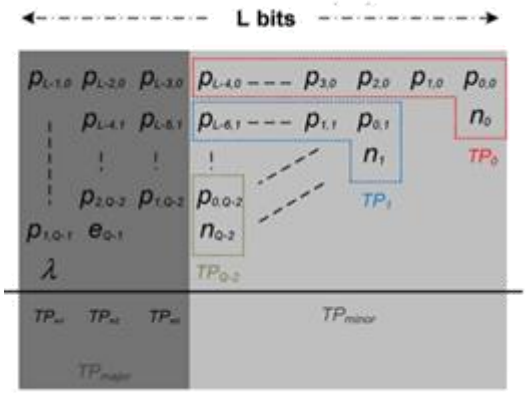
This table maps the partial products in the figure algorithms of L×L fixed width booth multipliers. The partial product array in Fig. 1(b) also can be divided into two parts: the main part (MP) including the most significant columns, and the truncation part (TP) including the least significant columns. Besides, the column information is included to adjust accuracy with respect to system requirements, it



a) Partition of truncation part with column information = 1



b)Partition of truncation part with column information=2



c) Partition of truncation part with column information=3

Fig Partition of truncation part with column information

Proposed Adaptive Conditional Probability Estimator (ACPE)

When fixed-width multiplication is concern, the quantized product can be expressed as follows:

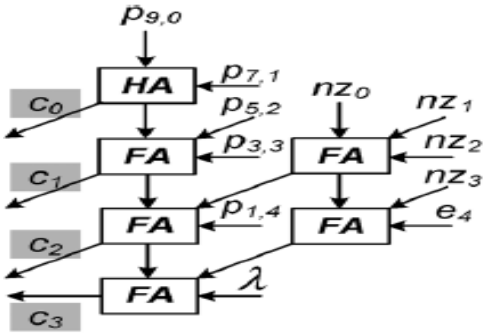
$$P = P_q = MP + TP$$

$$MP + \sigma . 2^{L}$$

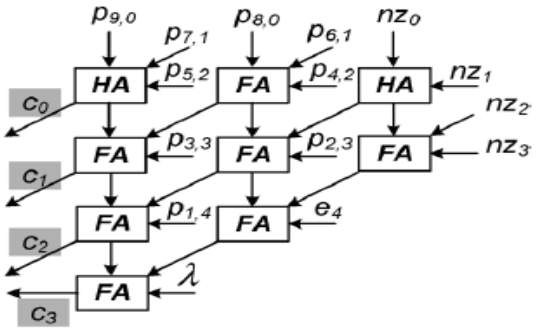
$$\sigma = [TP_{major} + TP_{minor}]$$

The TP $_{major}$ and TP $_{minor}$ are the major and the minor compensation part in TP,respectively. The TP $_{major}$ provides truly information to estimate ACPE, and the TP $_{minor}$ contributes compensation bias to MP based on conditional probability estimation. Therefore, the compensation bias can be calculated by obtaining TP $_{major}$ and estimating TP $_{minor}$.

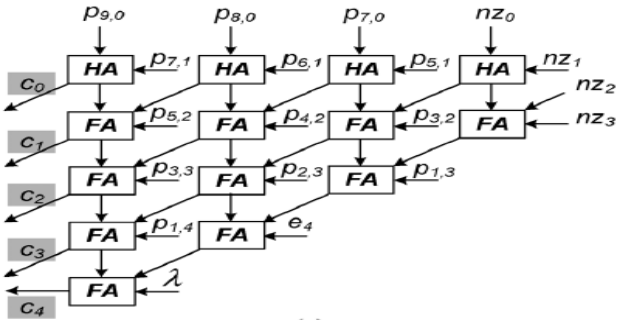
Compensation Circuits Of ACPE Booth Multiplier For Column Information



(a) Column information=1



(b) Column information=2



(c) Column information=3

Fig 4.2.3 Compensation Circuits Of ACPE Booth Multiplier

Architecture design of ACPE Booth Multiplier:

Based on the proposed ACPE formula the adaptive compensation bias can be calculated by obtaining word -length and column information . The architecture of the proposed ACPE Booth multiplier is designed by using tree-based carry save reduction followed by parallel-prefix carry-propagate addition architecture. According to the mapping Table, Booth encoder will generate the partial products. The compensation circuit is implemented to compute compensation bias and then the carry-save-adder (CSA) tree and parallel-prefix adder sum up the partial products of MP. The CSA tree is implemented by using the 4-2 or 3- compressor.

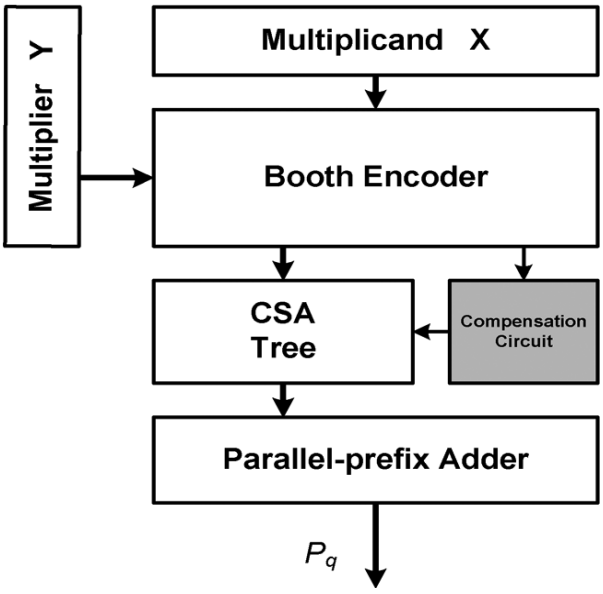


Fig 4.2.4 The whole architecture of the proposed ACPE Booth multiplier

Booth multiplier. Taking the large length as an example, the ACPE compensation circuit can be easily designed.

Application to 2-D DCT Computations:

The proposed ACPE Booth multipliers are then applied to a two-dimensional DCT for demonstrating the performance. The 2-D DCT core is implemented by a Shift-Register- Array and a one-dimensional (1-D) DCT kernel, which contains four 14-bit Booth multipliers. Therefore, the 10 test images, which are all 512 ×512 pixels with 8-bit 256 gray level data, are fed into the 2-D DCT to verify the accuracy performance. The system accuracy, defined as peak signal-to-noise-ratio (PSNR), and area cost are the important data for evaluating the performance of 2-D DCT.

CONCLUSION

In this paper, an Adaptive Conditional Probability Estimator is applied to fixed-width Booth multipliers. It is applied based on the theory called Conditional probability theory. Simulations been carried out. By using Xilinx ISE 8.1i the area and power can be determined. By comparing with the previous method, when the column information =1, the power has been considerably reduced upto 13.5% and the area has been reduced upto 37.6% . In the proposed method by varying the column information different values of area and power can be achieved. By varying the column information the power and the area can also be varied according to the system requirements.

RESULTS

INPUTS:

X : 01011001

Y : 01001101

SIMULATION:

SIMULATION RESULTS:

SIMULATION:

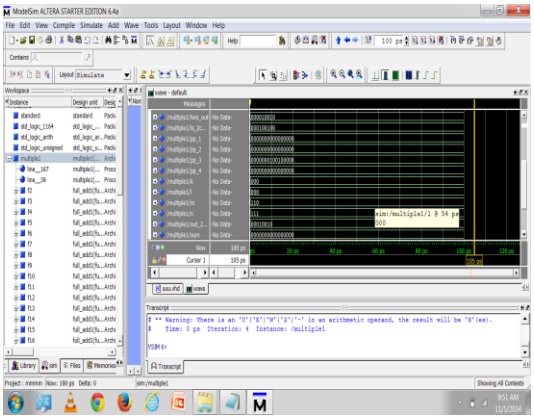


Fig :Simulation Result for Booth Multiplier

AREA

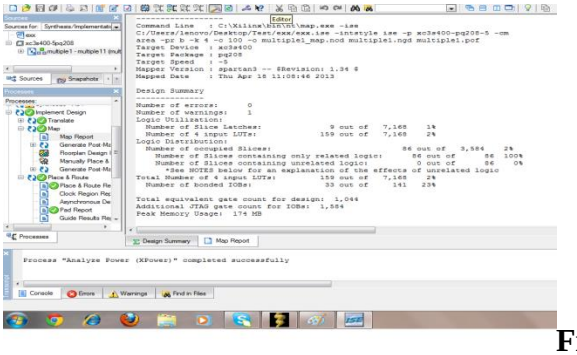


Fig :Area Of Booth Multiplier

POWER

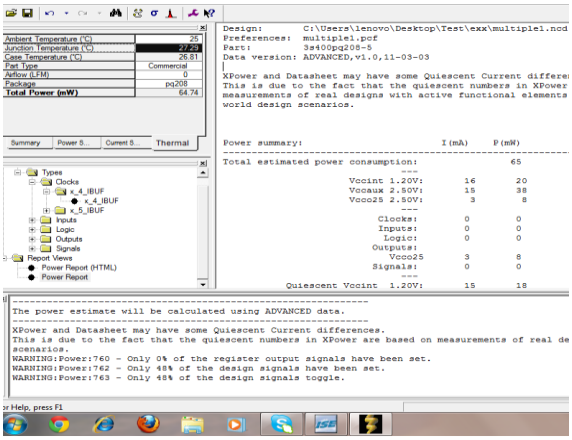


Fig: Power of Booth Multiplier

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