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Research Article

# An advanced state of art design of QCA based applications

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**ABSTRACT**
Quantum Dot Cellular Automata (QCA) offers a more efficient computational platform than CMOS. QCA is one of the most exemplary improvements proposed to replace the fundamental limitations of CMOS (complementary metal-oxide-semiconductor). It represents with circle type of dots digital information by polarizing electrons (polarization +1 and -1) and Quantum Dot. QCA technology can acquire a high density of integration in terms of clock frequency, smaller dimensions, high speed of operation (range of terahertz), and energy efficiency at the nanoscale level. In QCA, the implementation of Boolean logic functions uses an array of coupled quantum dots. We have a CMOS circuit in the existing model to overcome. This paper proposes a full adder circuit that is suitable for designing QCA-based circuits. The performance of various circuits based on the proposed full adder, full subtractor, half subtractor, and an Exclusive-OR (XOR) gate are verified using a truth table with a QCA Designer 2.0.3 tool to obtain computation results with graphical representation.

**Keywords:** Clocking phase; XOR gate; QCA Designer; polarization.

## Introduction

Quantum-Dot Cellular Automata (QCA) is one of the most cutting-edge approaches to draw circuit at the nanoscale. QCA aims to focus on Area and power because it uses less space in QCA to design any logic function. Because of smaller internal and external capacitance gets reduced. Since dynamic power consumption is directly proportional to capacitance, the power consumption is lower [1]. The Basic QCA cell has been shown in Fig. 1. Inside the cell, electrons can conform in four different ways, but they will only stay in the position that needs the least amount of energy. Furthermore, all electrons will adjust to the most significant possible distance between them [2]-[4]. The interaction between electrons is used to obtain the necessary logic states such as logic "0" and logic "1" by using electron functions. The cell polarization effect used to transfer logic from one cell to another. The charge configuration would be in degree the distribution of electronic charge in dots is measured by the polarization (P), which is given by the equation below [1]-[15].

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)} \quad (1)$$

The polarization persists to the end of the circuit, indicating no current flowing between the QCA cells. As a result, when a state change occurs from one logic to another, QCA circuits consume very little power [6]. The QCA wire structure is shown below in Figure. A QCA "wire" is a chain of cells that are physically attached. This type of wire binds various components. As a result, QCA will provide "processing-in-wire" services. QCA delivers a method for transmitting information without current flow since no electrons tunnel between cells [16]-[27].

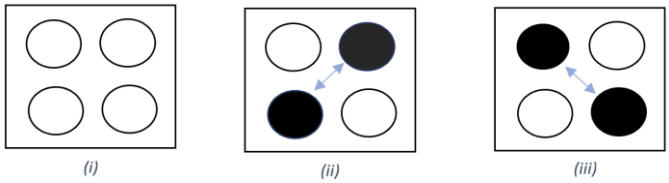



**Fig. 1. These are QCA cellexamples. (i) Empty (ii) Logic '1' (iii) Logic '0' [2].**

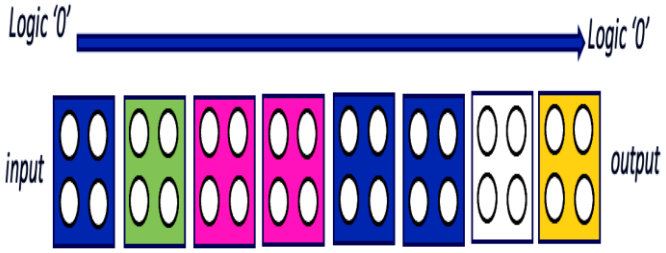



**Fig. 2. QCA Wire**

Figure 3 depicts the configuration of a QCA inverter and 3 input majority gates serving as the basic fundamental gates: To achieve inversion functionality, cells are placed diagonally from one another in an inverter. Five QCA cells make up a majority gate, which performs the following function [28].

$$M(a,b,c) = ab + bc + ac \qquad (2)$$

The most important structure is the three-input majority gate. The 3-input majority gate is essential and serves as an elementary gate since it is used to construct various logic structures such as gates and others. We can get AND Gate and OR gate by converting cell inputs to +1 to -1 polarization. The majority of gates can easily convert to AND or OR gates by having a fixed value for one input. For example, By setting either of the majority gates inputs to "0," an AND gate is formed:

$$AND(a,b) = M(a,b,0) = ab \qquad (3)$$

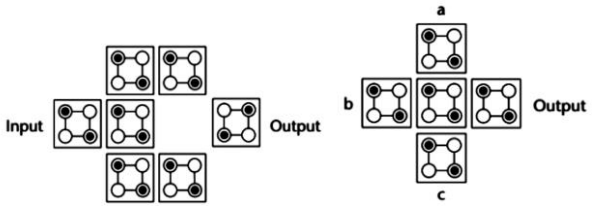
Likewise, to make an OR gate, set one of its inputs to "1":

$$OR(a,b) = M(a,b,1) = a + b \qquad (4)$$

In QCA, the clock is very relevant. The data flow of the direction in QCA design and energy to the QCA cells. The clock is divided into four phases, as shown in Fig. 4. One of the unique characteristics is in QCA's. It can create a different style of wire crossing. They are two types there (i) coplanar and multilayer crossover. Mainly it uses for the big circuit to understand the circuit neatly. Rarely use coplanar for the circuit [9]-[11]. Mainly used is multilayer crossover because it will understand. Fabrication of a semiconductor using GaAs. Four dots define a metallic gate. QCA devices are advanced-level fabrication used for existing CMOS technology. Two dots, also known as the half cell (capacitive coupled). The implementation of each cell is set up by a bistable simulation engine is known as a two-state system. It is described by is the Hamiltonian matrix $H_i$ [29]-[35].

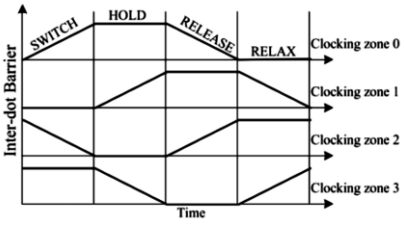
$$H_i = \begin{bmatrix} -\frac{1}{2} p_i E^k_{i,j} & -\gamma \\ \gamma & \frac{1}{2} p_j E^k_{i,j} \end{bmatrix} \qquad (5)$$

$P_j$= Polarization cell of j, $E^k$ is kinetic energy.

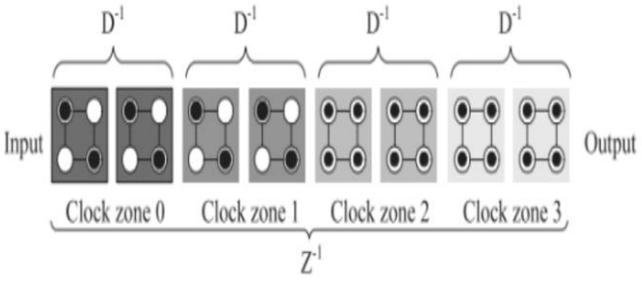



**(a) (b)**

**Fig. 3. QCA gates: (a) inverter, (b) majority gate [6]**




**(a)**




**(b)**

**Fig. 4. Clocking terms (a) types of clocking zones, (b) Clocked QCA wire.**

Each QCA clocking zone has four clocking phases; Fig. 4 shows a clocking zone with a 90° phase change from one to the next. QCA circuit clock signals are created using an electric field applied to the QCA cells to modulate the tunneling barrier between dots (i.e., the inter-dot barrier). CMOS circuits or carbon nano-tubes can produce an electric field. The cells are in the HOLD phase when the interdot barrier is solid, and they are in the RELAX phase when it is weak. As the inter-dot barrier moves from low to high or high to low, the cell is in the SWITCH or RELEASE phase. During the SWITCH process, information has transferred a cell latches during the HOLD phase. Since the cells in one clocking zone latch and remain that way until the cells in the next clocking zone latch, a clocked QCA "wire" can be thought of as a chain of D-latches. D-1, or a quarter of a clock cycle interval Z is a clocking zone delay (-1). In QCA, this is the smallest delay unit [36]-[43].

Section 1 describes the function of the QCA designer tool. Section 2 says the standard literature of work Section 3 of this presentation describes the proposed unique design of a full adder, including its schematic structure and truth table, and formulations. The construction of some combinational circuits using the proposed full adder and subtractor. The simulation results for obtaining graph output analysis also provided. Section 4 presents simulation results for seeing the structure and cell count, and Area in $um^2$. Simulation parameters and their values as determined by QCA Designer.

**Standard work of literature**

Quantum dot cellular automata proposed a method of complementary metal oxide semiconductor (CMOS) technology. Quantum dot cellular automata (QCA) is promising nanotechnology for high-performance integrated circuits as we are implementing our project on an advanced level controller in QCA. This QCA is one of the most powerful CMOS technologies at the nanoscale to design digital circuits. It represents by a polarization of electrons. QCA has optimistic advantages over CMOS technologies. It made even more attractive for its size, faster speed, feature, high performance, level of the complex, low power consumption than CMOS technology.

In the existing model, we used CMOS technology. CMOS technology used in serval key like in microprocessor, digital sensor etc. In 1963 the first frank wan lass invented the CMOS technology. In VLSI technology has billion of the transistor in integrated into one chip. One of the disadvantages of CMOS is short circuit power. It happens because, at the time, both CMOS and NMOS gets on at the same time. Another disadvantage of CMOS is setting more input transition time. We have converted from NMOS only to CMOS technology. In order to avoid static power consumption in CMOS, we will get almost zero static power consumption because there will be no direct path from $V_{DD}$ to GND. One of the main reason to move from CMOS technology is to have a better noise margin. CMOS technology total power calculated as the sum of dynamic power.

$$Total\ power = Dynamic\ power + Leakage\ Power$$

$$Dynamic\ power = CV^2 f \qquad (6)$$

Where, C = Capacitance time, V = Voltage of operation, f = frequency of operation.

In CMOS, most of the power consumption because of dynamic power. Mostly, 80% of power because of dynamic power. CMOS is a technology that uses integration timing MOSFET in order to accommodate more space. The design includes cellular-shaped with four quantum dots and two excess electrons. It has significant benefits, and this is performed. In circuits in CMOS, we have difficulty implementing and practicable. From this situation, we are a QCA designer tool. We followed the objective in our design we are assuming to minimum complexity and number of cell. The design and implementation are done in the QCA designer tool. It represents binary is '0' and '1', which propagate from input to output. All designs are implemented in the QCA tool.

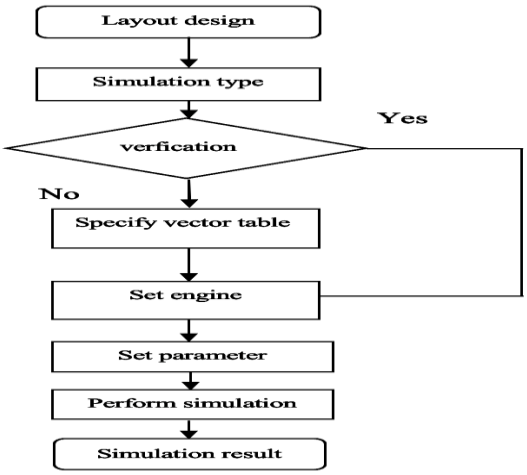



**Fig. 5. Complete structure of the QCA tool.**

**Design aspect of adder and subtractor**

In the proposed model, we are implementing adder and subtractor using the QCA tool. In QCA, we don't need any transistor and capacitor, and resistor to build the circuit in it. So we were working on it. In the future, most of the member will use this QCA designer tool.

**A. Exclusive -Or (XOR) Gate**

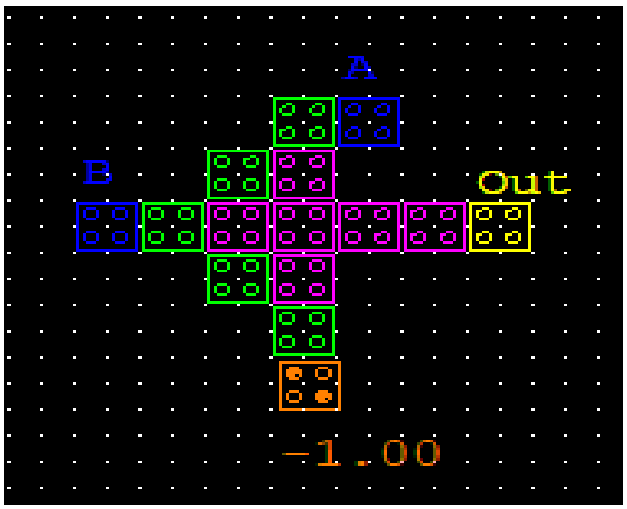



**Fig. 6. QCA design of XOR gate.**

We have seen three principal gates like AND Gate, The OR Gate and The NOT Gate. They are two "hybrid" logic gate called the exclusive-OR Gate and its complement the exclusive-NOR Gate. The digital logic gate gives an actual output when the input is odd. XOR Gate is known as exclusive – OR gate. It is a logic circuit that produces a logic high output when both the inputs are different (logic 1). When both the inputs are the same, it makes a logic low output, i.e. (logic 0) the expression of XOR gate.

**B. Half Subtractor**

It also a combinational circuits which contain two bits. It consists of two inputs and two outputs (D, Bout). Its designs have the A-B, not A-B since $B_{out}$ then becomes $B_{out} = \overline{A}B$ Subtractor is not commutative, but Ds difference is calculated using a XOR gate which is commutative.

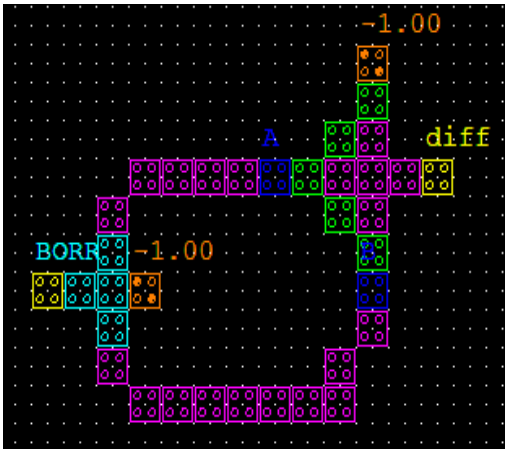



**Fig. 7. QCA design of half subtractor.**

**C. Full Subtractor**

It is a combinational circuit. To perform, so we use the three inputs (A, B, $B_{in}$) and two outputs (differ, borrow). It is the combination of two half subtractor. The half subtractor and full subtractor generate the borrow out it needs to borrow from the next digit. It was being subtracted from B and $B_{in}$ from A. In full subtractor schematic design have XOR, AND, NOT, OR logic is used. In QCA design, also we used XOR, AND are used.

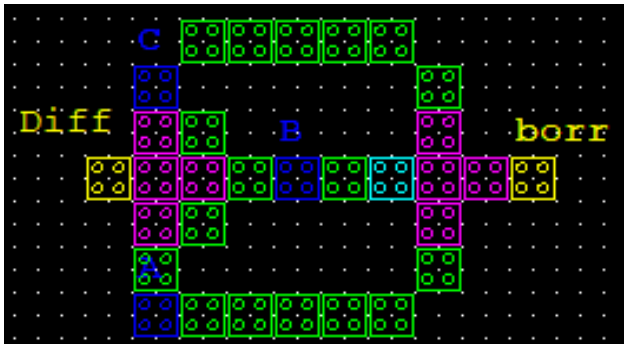



**Fig. 8. QCA design of full subtractor.**

**D.** Full adder

C. S. Lent et al. was designed the first QCA full adder in 1994 without a clocking term. But in this, we are using clocking term into it to design a full adder. For those conditions, one clock term has used.

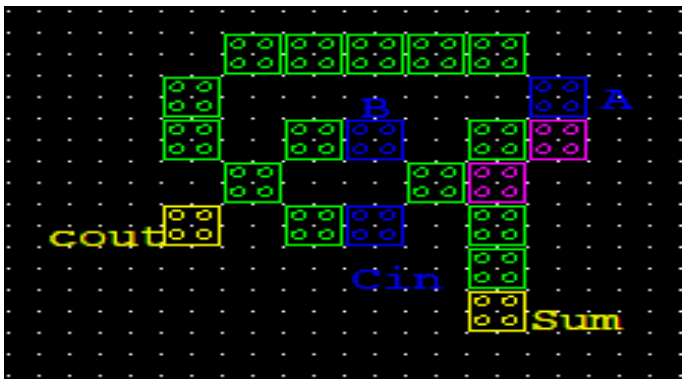



**Fig. 9. QCA implement of full adder circuit.**

Full adder is implemented with logic operations. Full adder has three input and two output. A full adder can be constructed by using two half adder. Full adder consists of XOR gate, And and or gate. Mostly ALU is consist of the adder. Adder design with XOR Gate, which is a power-hungry gate. The probability which switches of XOR Gate ¼. Whatever might input the probability of switch activity of these XOR gates fixed that is ¼ in CMOS because of this XOR power-hungry they might more power consumption. So, in

order to overcome the power consumption problem, we have moved to QCA.

**Result Analysis of proposed model**

The performance and other characteristics of the designs will be observed in the QCA designer tool.

**Table 1: parameter of different circuits**

| Parameter name | Values |
|---|---|
| No. of samples | 12800 |
| Convergence tolerance | 0.00100 |
| Radius of effect | 65.000 |
| Relative permittivity | 12.900 |
| Clock high | 9.800e-022 |
| Clock low | 3.800e-0 |
| Clock shift | 0.00e+000 |
| Clock amplitude factor | 2.000 |
| Layer separation | 11.500 |
| Max iterations per sample | 100 |

The simulation result is correct, but some delay occurred in some circuits.

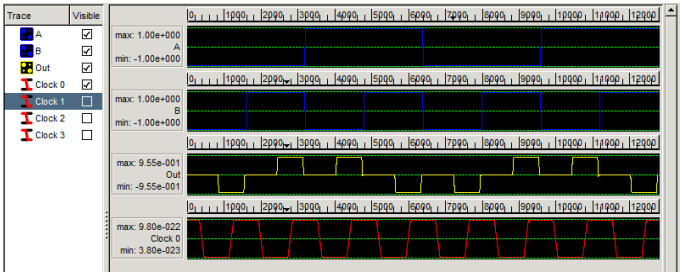


**Fig. 10. This is the output of Ex-Or Gate Figure 7**

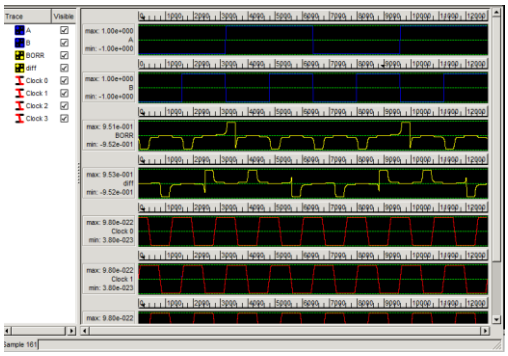


**Fig. 11. It is an output of half subtractor of a Figure (9)**

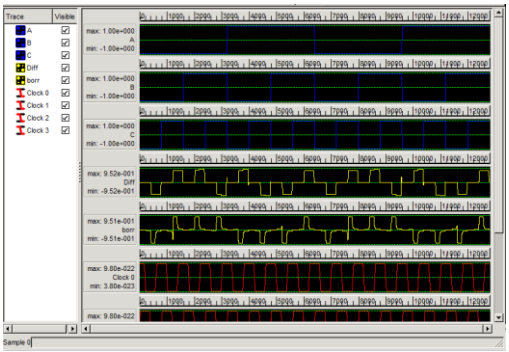


**Fig. 12. It is an output of the full subtractor of a Fig. 11.**

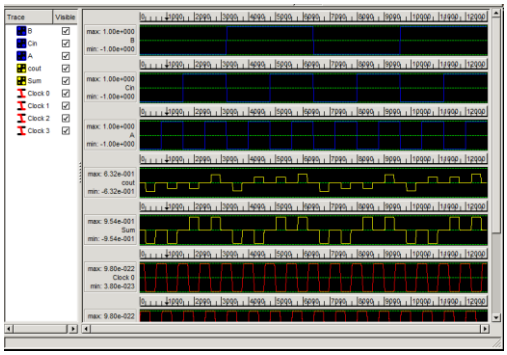


**Fig. 13. The simulation result of the full adder (Fig. 13) in the QCA designer tool.**

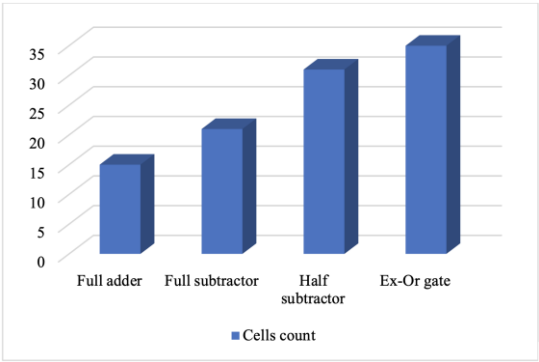



**Fig. 14. Cell count of individual design.**

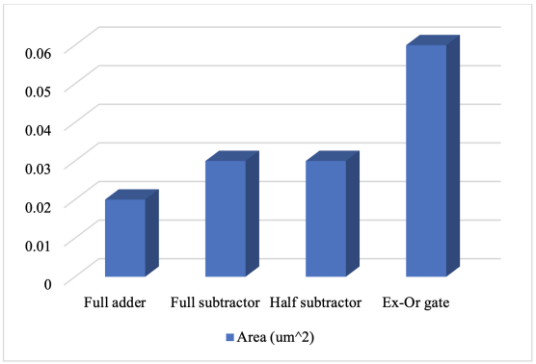



**Fig. 15. Show the size or Area of the design circuit.**

**Table 2: The Result of Circuits is Performed in QCA.**

| Circuits | Total cells | Area ($um^2$) |
|---|---|---|
| Ex-or gate | 15 | $0.02um^2$ |
| Full adder | 21 | $0.03um^2$ |
| Full subtractor | 31 | $0.03um^2$ |
| Half Subtractor | 35 | $0.06um^2$ |

### E. Future scope

Design more and more circuits with complexity and high speed. In future, obtain new circuits with this tool in the future. It has capable of doing the problematic circuit quickly. In this software, presently do with two dots and four dots and eight dots.

### Conclusion

In this paper, QCA software is used. This is a new technology at the nanoscale (1ns) circuit suitable for designing high-performance logic circuits. This design has less power consumption, area, time in these circuits. These QCA circuits are better than CMOS technology. The CMOS technology contains more size, more time, high power consumption. We are using an alternative like the QCA tool to make sure circuits can handle at high speed, less complex etc., various circuits like the full adder, full subtractor, XOR gate. The output is verified with a truth table of the different circuits that have to be acquired using the

tool. We used four dots implement for all circuit with a clock cycle pulse. In clock cycle has a different time frame. By using the QCA tool, all design has been implemented and the accurate and reliable results. The existing work and proposed models have analyzed the circuits. In circuits like full adder have acquired about improvement in cell count. The designed circuit and simulation result shows the proposal QCA based circuit to minimize QCA cells and minimize Area size.

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