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Research Article

Energy Harvesting Digital Filter Implementation With Novel Architecutre

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ABSTRACT

In VLSI, for performing multiplication, we use a*b. We use the booth multiplication mechanism rather than the standard conventional method to improve the speed since it generally requires lower power, area and reduces delay. Some bits overlap with each other during the multiplication process in the convectional multiplication method (whereas booth multipliers consist of shifting process), making the system more complex and decreasing output efficiency. To overcome this, SPST is implemented such that unwanted transactions are neglected and also eliminate the overlapping bits. This affects the carry changes and data generation parts and even reduces the unwanted power flow in adders. It uses Radix 4 multiplier, which requires addition processors. In the previous multipliers usage of Ripple carry adder, Carry save adder, carry ahead adder, which are the basic types of serial adders where they utilize serial adding mechanism where the data is processed bit by bit that make the system more complicated. To reduce these problems, we are using parallel prefix adders that work in a higher speed manner, which uses carry propagation and carry generation internally to perform additional operations and improve speed. So, this project is implemented in VLSI prototype with respect to Xilinx ISE software and Verilog programming language.

Keywords: Booth multiplier; Spurious power suppression technique (SPST); Booth Multiplication; digital signal processing (DSP); Modified booth multiplier; Pre-Fix Parallel Adders.

Introduction

Multiplication is undoubtedly a principal operation when considering some of the advanced concepts like machine learning, neural networks and digital signal processing. It is reasonable to use an enhanced multiplier for such applications. In many digital signal processing applications, the high performance of the multipliers is a critical acceptance criterion. Multipliers are salient components of numerous high-performance systems in which complex arithmetic operations occur, such as FIR filters and digitally processing a signal, including primitive operation systems like calculator, microprocessor and many more. The overall performance of such systems and circuits relies on the multiplier functionality, so it is only coherent to use the best of the multiplier, which has enhanced speed, lower power consumption, moderate area, and persistent delays [1]-[23].

However, most multipliers have longer time delays, large area and greater power consumption so it is crucial to design a multiplier with enhanced properties. There are multiple ways to perform multiplication in digital circuits. Some of them are parallel-parallel, serial-serial, serial-parallel and parallel-serial, and many proposed methods and designs to amplify the multiplier power and speed of the multiplier. Using conventional and straightforward multipliers for DSP systems and other technologies comes with a challenge, and that is, the multiplier coefficients are not constant. Had it been the case, it would've been easy to lessen the consumption of power using a generic multiplier with a network of shift adders and shift subtractors, but it comes with its own set of challenges. One of the downsides is the inflexibility of the simplified multiplier during multiplication operations with varying coefficients. However, to overcome this challenge and to improve the ability to process.

Several reconfigurable multiplier techniques capable of supporting multiple-precision multiplications are developed to achieve improved processing ability. Advanced VLSI technology has enabled designers to introduce a large number of complex modules, which was previously inaccessible. There have been several high-speed multipliers attempted and implemented. The improved booths algorithm with Wallace tree at higher radixes are broadly acknowledged as a high-performance algorithm for general problems, but it can still be optimized.

A.Objective

This research provides a radix-4 multiplier with two speeds for accelerating optical filters, artificial neural networks, and other algorithms used for machine learning, [1][4]. So, therefore, we introduced improved multiplier architecture of high-speed arithmetic operations by using an enhanced two-speed, radix-4 multiplier using the spurious power suppression technique. This technique enables us to keep in check the significant multiplier. This technique works by increasing the density of bits of operands by using a modified array for sign extension. The various components used in this proposed model are the enhanced algorithms of different multipliers and adders. It mainly uses the modified booth multiplier with the radix-4 scheme to improve the speed of operation. SPST essentially uses a parallel-prefix adder to improve the power consumption as an add-on [24]-[35].

B. Booth Algorithm

Using Radix-2 andrew donald booth first implemented the booth algorithm in 1950. Booth's algorithm is an efficient and quickest method for realizing a digital circuit that multiplies two binary numbers using two's complement notation in hardware. Booth multiplication allows for smaller and speedier multiplication circuits, and it is achieved by recording the multiplied numbers. These booth multipliers are commonly used in ASIC based applications due to their higher computing speed and smaller size. The numbers, known as bits, of the binary number system are 0 and 1. For every binary integer is multiplied by a binary bit, the result is either 0 or the original number. This improves the efficiency and functionality of partial product creation. However, the generation of partial products largely depends on the type of radix scheme and recording algorithm used. For example, it could be radix-2 or radix-4 encoding. Booth's recording is a very effective means of producing partial products since it uses the booth algorithm to produce multiplication for a group of consecutive binary bits. As a result, this radix-scheme generates fewer partial products, resulting in lower power and area than the normal booth multiplier. Fig. 1 shows the structure of booth multiplier [36]-[43].

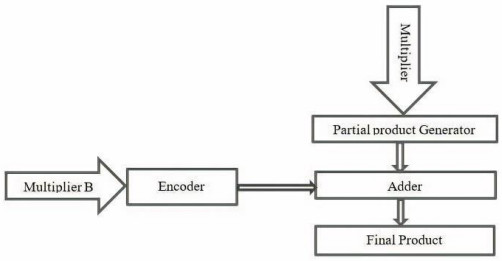

Fig. 1. Booth multiplier Architecture.

Table 1: Booth Encoding Table

Yi	Yi-1	Zi-1	Value of the multiplier	Case
0	0	0	0	String of 0s
0	1	1	+1	String 1s end
1	0	1	-1	String 1s start
1	1	0	0	String of 1s

C. Radix-2 procedure

The Radix-2 scheme involves adding 0 to the multiplier's LSB and pairing two from left to right as a primary step, and then if it's 00 and 11, no operation is done according to the encoding as described in Table 1. If it's 01, it indicates the end of the string of 1's. It multiplies the partial product by multiplicand and, if multiplicand is 10, indents the partial products by subtracting the multiplicand from the 1's series' beginning as shown in Table 2.

Table 2: Example of radix-2 Multiplication

A		1 0 1 0	-6
X	x	1 $\bar{1}$ 0 $\bar{1}$	-3
Y		0 1 0 $\bar{1}$	recorded multiplier
Add -A		0 1 1 0	
Shift		0 0 1 1 0	
Add A		1 0 1 0	
		1 1 0 1 0	
Shift		1 1 1 0 1 0	
Add -A		0 1 1 0	
		0 1 0 0 1 0	
Shift		0 0 1 0 0 1 0	

D. Modified Booth Algorithm

Table 3: Modified Booth Multiplier Radix-4 Encoding

Xi	Xi-1	Xi-1	Yi	Yi	Operation	Case
0	0	0	0	0	+0	0's string
0	1	0	0	1	+A	One
1	0	0	$\bar{1}$	0	-2A	1's begins
1	1	0	0	$\bar{1}$	-A	1's begins
0	0	1	0	1	+A	1's end
0	1	1	1	0	+2A	1's end
1	0	1	0	$\bar{1}$	-A	Zero
1	1	1	0	0	+0	1's string

In radix-4, there have been some significant disadvantages of using booth multiplier with the radix-2 scheme, and using an enhanced booth multiplier with radix-4 can overcome the challenges. This modified booth algorithm can bring down the number of partial products by half in multipliers using 3-bits simultaneously, unlike the radix-2 multiplier, using a technique called overlapping technique. The grouping then begins with the LSB, with the first block containing just two bits of multipliers and 0 for the third bit. By recording the multiplied numbers, the modified booth algorithm makes for a smaller and faster circuit. Table 3 is used as an example here.

E. Radix-4 Algorithm

If required, extend the sign bit 1 location to ensure that n is even. To the right of the multiplier's LSB, add a 0. Each partial product would be 0, +y, –y, +2y, or –2y based on the value of each vector. The 2's complement is used to create negative y values, and carry look ahead (CLA) quick adders are used. The multiplication of y is accomplished by moving y to the left by one bit. In any case, only n/2 partial products are produced while designing n-bit parallel multipliers. This approach has the benefit of halving the number of partial products. This approach has the benefit of halving the number of partial products. This is important in circuit design because it affects the circuit's propagation delay and the complexity and power usage of its implementation. Refer to Table 2 for details.

Table 3: Example of Radix-4 Multiplication

A			00	01	11		7
X	x		11	01	11		-9
Y			01	10	01		record multiplier operation
			-A	+2A	-A		
Add -A	+		11	10	01		
2-bit shift		1	11	11	10	01	
Add 2A	+	0	00	11	10		
			00	11	00	01	
2-bit shift			00	00	11	11	01
Add -A	+		11	10	01		
			11	11	00	00	01 -63

F. Parallel-Prefix Adder

Group generate means that a bit within the range generating an output carry, and generated output carry propagates through the end of the range. Everything within the range of propagation is termed group propagate. If we combine the ranges using a dot operator, they produce the range that is the summation of two ranges, and the combined range has to fit without any gaps to generate an output.

Our primary focus is to calculate when the operation of an adder is done. It can be termed completed when it has estimated all the carry outs for all the positions. The adder can produce a carry out at the current bit position when it has available group propagates and group generates range from point 0 and can be done using only the carry in's. In the later part of this paper, we have shown the kogge's stone adders operation using the same principle.

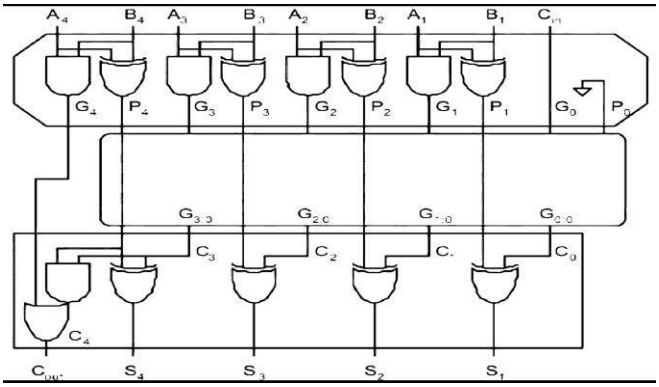

Fig. 2. Parallel- Prefix Adder

From Fig. 2, parallel prefix adder is one of the most important components of digital networks are adder arithmetic units [3]. Any improvement in binary addition will result in performance improvement for DSP applications. The key problem with binary addition is that as the input width increases, the length of the carry chain increases as well, resulting in a prolonged period of time to generate output. The PPAs compute a segmented series of intermediate prefixes before locating large group prefixes before all of the bits are computed, as described in [3]. Since the calculation is performed in these systems are in parallel, the results are fast.

One of the most significant adders for arithmetic operations is the carry select adder. It's a high-speed adder used in VLSI architectures, but it comes at the expense of space and power [2]. A 16-bit carry pick adder based on the brent kung adder has a smaller chip footprint, a marginally longer latency, and is a more powerful high-speed adder than other CSLA architectures. The same has been found through simulation, which is discussed further in the proposed model. The BKA structure has a sparse network that takes up less space than the KSA structure but has more logic depth. While KSA has better overall performance than other PPAs due to its lower hardware complexity, the proposed research work has introduced and compared other PPA structures such as Han-Carlson (HCA), Brent-Kung (BKA), and ladner fischer (LDA) for better performance in terms of the number of cells used, delay, or power consumption [3].

G. Brent Kung Adder and Ladner Fischer Adder

Brent Kung adder is a carry-lookahead adder of the form parallel prefix adder. BKA relatively performs well compared to other parallel prefix adders and has less chip area, enabling us to use it for multiple applications. In addition to it, it is much faster than a ripple carry adder. The brent–kung adder is much

easier to build than the kogge–stone adder since it needs fewer modules to execute. It also has a lot fewer connections to other units, which adds to its ease of use. However, due to its disadvantage being significant, kogge stone adder is preferred. Fan-out is one of this adder's significant drawbacks. The present propagating through the adder can be broken and weakened as a result of fan-out.

The carry is measured in parallel in brent–kung adders, which significantly reduces the additional time. Brent–kung adders and other parallel adders have been improved to minimize power consumption and chip area while increasing rpm, making them ideal for low-power designs.

One of the parallel prefix adders is the Ladner–fischer adder. This LFA is used to improve the speed of arithmetic operation. This helps remove the delay that occurs during the propagation of carry, which is a significant disadvantage of ripple carry adder that can be overcome using LFA. This type of adder is used explicitly for extending the performance efficiency that executes the addition operation. The extension process is performed by the Ladner-fischer adder, which is a parallel prefix adder. It is divided into three stages: pre- processing, propagation and generation, and post-propagation. To execute the arithmetic operation, it appears to be a tree structure. The Ladner-fischer adder is made up of grey and black cells. Two AND gates and one OR gate make up each black cell. There is only one AND gate in each grey cell.

Proposed Models

A. SPST based TSM Model

The architecture of the given SPST based TSM, as shown in Fig. 3, shows that the TSM model is divided into two sub- circuits, each of which has critical pathways T and KT. The frequency at which the multiplier operates is (1/T), with a critical path of KT in the fully combinational region KT.

We must know, K value mentioned in the equations is the ratio of the two sub- circuits' delays. K' refers to the number of clock cycles required for addition operation, after which the result is stored in the product register P. Now we must check the booth encoding bits before doing the addition operation, i.e., the 3 LSB bits of product P for the two cases shown: 1) the output regarding the partial product and booth encoding are 0x and zero. 2) The output regarding booth encoding is non-zero.

Skip = {1, if P [2:0] E {000,111): 0, otherwise} (1)

Considering (1), when all the encoded value is either zeroes or ones, the skip value (mentioned in Fig. 3) is equal to 1 otherwise skip equal to 0. Only right shift and accumulation operations are accomplished by clocking the design K times at T for a skip value of 1 with a critical path T. The two speed multiplier's total delay can be calculated using (2), where O denotes the number of non-zero encodings.

T (0) = (N-0) T + 0K'T (2)

The lower bound, O=0 and upper bound, O=N limit for the total delay is calculated using (3).

NT <= T <= NK'T (3)

In case of trying to improve the performance delay following two optimizations can be performed in the standard TSM architecture. In the first case, following Fig. 3 the product is now not obtained from the product register P and instead it is considered from the shifter block. The product is now produced in one less clock cycle as a result of this adjustment in the operation. The control circuit's counter now increments log2(N) rather than log2(n)+1. In the second scenario, the control circuit is optimized by removing the counter 2 and comparator from the control circuit.

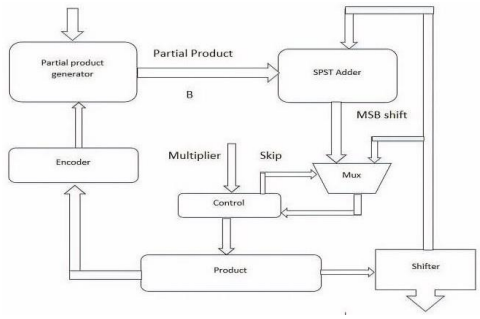

Fig. 3. n-bit proposed SPST based TSM architecture

B. Kogge-Stone Adder

Before going into our proposed model, which is the Modified Kogge-stone adder (MKSA) let us discuss in brief Kogge-stone Adder and its properties to get a better idea about the topic. The Kogge-stone adder falls into the category of parallel prefix adders as it is meant to generate and propagate signals in advance compared to other adders, which results in a better performance and is so considered among the fastest adder in current times. There are several components inside this adder, such as generate propagate block, grey cells, black cells, and buffers. Along with the Kogge-stone adder, let us mention some more parallel prefix adders such as Brent-Kung adder, Han-

carlson adder, and a faster version knows as the Lynch-swartzlander spanning tree adder. The Kogge-Stone adder usually needs more area for functioning as compared to the Brent-kung adder, but comparatively, the fan-out (in digital electronics, fan-out is the total number of gate inputs driven by the output of another single logic gate) at each stage in KSA is lower. However, due to the use of too many wires, congestion takes place, which is a common problem in KSA. There are three processing stages in the Kogge-stone adder for calculating the sum bits. These stages are referred to as; 1. Pre-processing stage. 2. Carry generation (PG) network. 3. Post-processing stage.

C. Modified Kogge-Stone Adder

In the above-discussed situation, KSA is a complicated setup, so it requires a larger area for better functioning, so in to reduce the hardware complexity while trying to maintain or enhance the performance level, the second stage is altered in MKSA shown in Fig. 5 to create a modified version of the actual Kogge-Stone adder. The Kogge-Stone adder shown in Fig:4 is comparatively quicker than the other known parallel prefix adders mentioned above as the KSA consists of a fan-out of 2 in every stage. In order to try and simplify the computation in KSA, we can remove the redundant cells in order to compensate for the increased delay. We can modify the Kogge-stone adder by eliminating the black cells as shown in Fig. 6, and then the wiring connections are rerouted to compensate for the working of the adder. In Fig. 4 the propagate-generate network section of the 8-bit MKSA is displayed. Usually, there is a delay in MKSA, which can also be reduced by rerouting the second stage's wired connection. Still, this process is not very useful and practical as the area for the operation of KSA does not change. In order to increase the speed of the adder, we can remove the redundant black cells, and in this process, we can reduce the area of the adder.

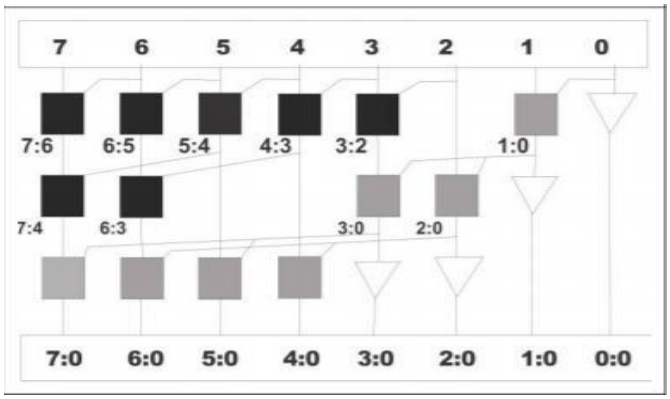

Fig. 4. PG network section of modified kogge-stone adder.

Thus, the MKSA is built which reduces the area required for operation and increases the speed of the adder. Compared to the KSA (Fig. 4), the MKSA gives an overall improvement where the area is reduced by 26.9% and power dissipation is reduced by 23%.

B. Brent Kung Adder

Simulation Results and Experimental Findings of the Proposed Work

A. Simulation Outcomes

The proposed model or design has been simulated on Xilinx software tool. The output of the multiplier circuit used in the design is shown in the below figures.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	2065	204000	1%
Number of fully used LUT-FF pairs	0	2065	0%
Number of bonded IOBs	128	600	21%

Fig. 5. Device Utilization Summary of Brent Kung Adder

C. Ladner-Fischer Adder

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	2065	204000	1%
Number of fully used LUT-FF pairs	0	2065	0%
Number of bonded IOBs	128	600	21%

Fig. 6. Device Utilization Summary of Ladner Fischer Adder

D. Modified Kogge-Stone Adder

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	2049	204000	1%
Number of fully used LUT-FF pairs	0	2049	0%
Number of bonded IOBs	128	600	21%

Fig. 7. Device Utilization Summary of Modified Kogge- Stone Adder

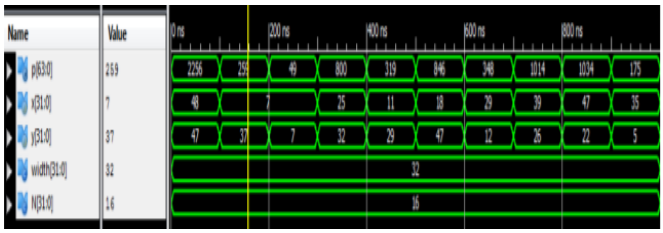

Fig. 8. Simulation Outcome of MKSA.

E. Modified Kogge-Stone Adder

From Fig. 7 and Fig. 8, we get the device utilization summary of brent kung adder and ladner-fischer adder. From Fig. 9, we get the device utilization summary of modified kogge-stone adder. Fig. 10 gives simulation outcome of the proposed model i.e. modified kogge-stone adder.

Table II. Delay Summary and Power Summary of different PPA's

PPA Adders	Delay Summary (ns)	Power Summary (W)
BKA	27.878	1.065
LDA	27.878	0.165
MKSA	25.903	0.065

Table 2 shows the comparison between the delay and outcomes of various parallel prefix adders (PPA).

Conclusion

This paper here refers to a modified Two-Speed Radix-4 multiplier using the spurious power suppression technique (SPST) to lower the power consumptions. Compared to a standard two-speed multiplier, the 64-bit input modified version shows specific improvements such as the power consumption are reduced by 7.97%, and latency is improved by 28.44%. Also, it has a better performance record compared to other multipliers in terms of PDP for each input-bit configuration. So, in short, the TSM, which SPST improves the power delay, reduces computation time in several applications. In the future, work will be done to utilize the specified SPST based TSM in low power, high-performance applications. Also, we have learnt that among all the current parallel prefix adders, the Kogge-stone adder is simply a faster version that can also be modified in a certain way to improve overall performance, which includes removing the redundant black cells and re-arranging the wiring connections to increase the adder speed and also reduce its area. Further modifications will be done in future to improve its performance in a more efficient manner to get better results.

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