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Research Article

Advanced Transistor Nodes: Basic module realization for data security

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ABSTRACT
In this research paper, we planned a low leakage power and high speed decoder for memory cluster application and proposed modern four strategies. In this paper, the collation of source predisposition decoder, source coupling decoder, body bias decoder and cluster decoder are planned and analyzed for memory cluster application. The plan is recreated utilizing Cadence virtuoso with 20nm innovation. The parameters of 3 to 8 decoders designed at 20 nm FinFET nodes using Cadence Virtuoso.

Keywords: Body Biasing; Decoder; FinFET; Source Biasing.

Introduction

The increase in demand of ultra-high-speed processors, lower power consumptions of integrated circuits and smaller dimensions has evolved the technology scaling and challenging issues for the designers. FinFET built on single walled semiconducting are been leading to complement Silicon and extended CMOS technology scaling at sub-18nm technology nodes [1]-[14].

The FinFETs was introduced by Tans to demonstrate a specialized switching ways and made the FinFETs in research progressions. In earlier FiNFETs are back ended that involves the design of strips parallelly on a metal over a silicon diode substrate in random pattern depositing silicon on top. The FinFETs of two metal strips ae formed consists of the preconditions of field effect transistor. The metal strip one is 'source' and second is 'drain' makes the contact ends. A metal contact is made on back which is used as gate oxide is of silicon oxide substrate [15]-[23].

To increase the device performance FinFET has designed with top-gated structure. The structure is made by using FinFET on oxidized wafer. High resolution beam lithography is used to isolate source and drain contacts. At the top of the nano tube a thin top-gate dielectric is deposited by using atomic layer deposition or evaporation. Eventually the top gate contact on gate dielectric [24]-[29].

In the design process the combinational circuit is considered that is the binary decoder which is a combinational logic circuit that converts n coded binary inputs to the 2n outputs. The combinational circuits have many applications like data multiplexing, demultiplexing, seven segment display, encoder and memory address decoding [30]-[36].

In the VLSI system power consumption is an important consideration. Here is the normal 3:8 decoder constructed using NAND gate and for the complimentary operation Inverter test bench is used. There are different colors used for indicating the terminals. The ground terminal is indicated by green color line, Vdd terminal is indicated by pink color line. The A, B, C are the inputs and the DO to D7 are output terminals indicated by blue colors [37]-[39].

The 3:8 decoder is constructed using NAND gate and for the complementary operation inverter test bench is used, the operation of decoder is when the input is ABC=100 the D3 line becomes zero NAND all other lines become one. The leakage current is reduced by connecting a sleep transistor with NAND gate.

The cluster technique is used in the conventional circuits because here sleep transistors are not used instead of that a common gate is utilized which is associated among all NAND gates to the ground terminal. This method is utilized to decrease the region and to work the decoder as same as ordinary decoder.

Proposed Circuit: Design and Realization

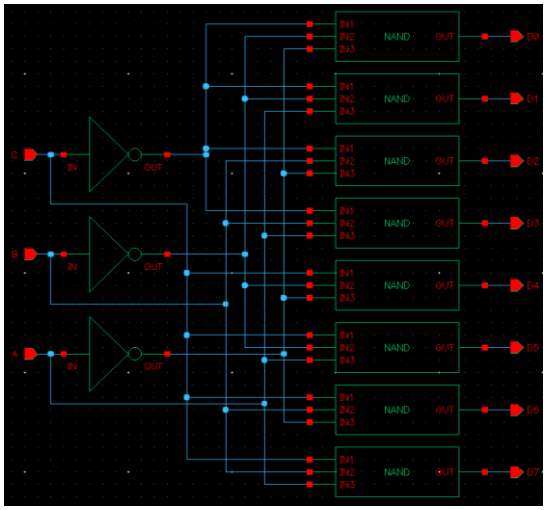

Fig. 1. Decoder block diagram using NAND gates.

Considered that is the binary decoder as shown in Fig. 1, which is a combinational logic circuit that converts n coded binary inputs to the 2n outputs. The combinational circuits have many applications like data multiplexing, demultiplexing, seven segment display, encoder and memory address decoding.

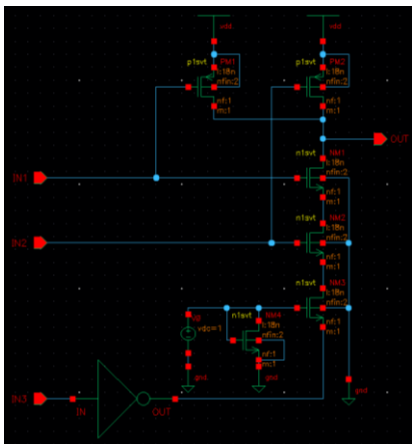

Fig. 2. Source coupling NAND circuit.

In the VLSI system power consumption is an important consideration. Here is the normal by using NAND gates 3:8 decoder is designed. for the complimentary operation Inverter test bench is used. Source coupling NAND gate is represented in Fig. 2 and the three input NAND is given in Fig. 3.

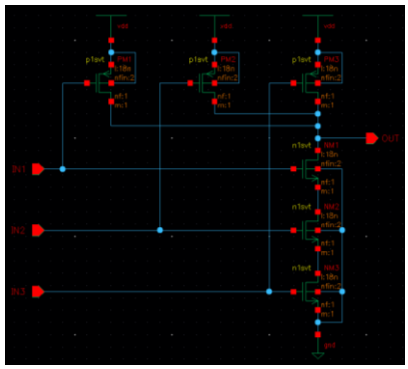

Fig. 3. Schematic of 3-input NAND gate.

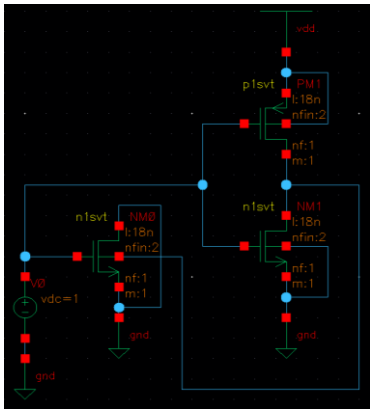

Fig. 4. Body biasing technique.

The 3:8 decoder is constructed using NAND gate and for the complementary operation inverter test bench is used, the operation of decoder is when the input is ABC=100 the D3 line becomes zero NAND all other lines become one. The leakage current is reduced by connecting a sleep transistor with NAND gate as shown in Fig. 4.

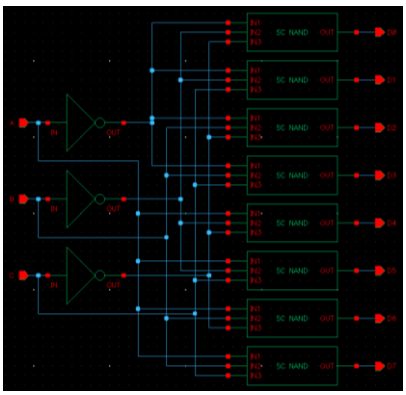

Fig. 5. Block diagram of 3 to 8 decoder using source coupled NAND gates.

The cluster technique is used in the conventional circuits because here sleep transistors are not used instead of that a common gate is used which is connected among all NAND gates to the ground terminal. This technique is used to reduce the area and to work the decoder as same as normal decoder.

The circuit is like the cluster circuit the one difference is body biasing circuit is used instead of sleep transistor. The Threshold voltage of the transistor is modified by the body terminal of the biasing circuit.

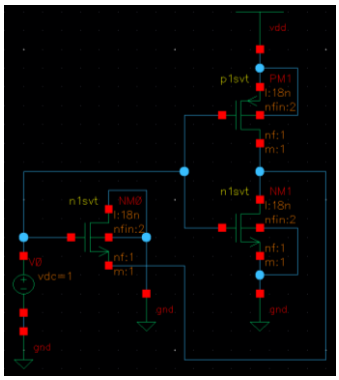

Fig. 6. Source biasing circuit.

In the above circuit source bias circuit is used instead of sleep transistor. The common input is connected to the voltage supply, the output of inverter is connected to the source terminal and the body terminal is grounded. Sleep transistor threshold voltage is used to

control the source terminal which in turn controls the output of invertor circuit.
This source coupled strategy the third terminal of NAND gate is associated to the inverter circuit input, source terminal of NMOS is associated to inverter circuit.

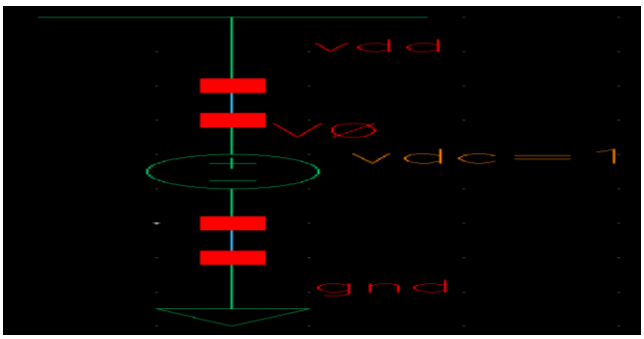

Fig. 7. Biasing without any sleep transistor.

Design of Efficient Decoder circuit consists of following techniques:

- The Decoder circuit designed without utilizing sleep transistor using NAND gate
- The Decoder circuit designed utilizing sleep transistor using NAND gate
- The Decoder circuit designed utilizing Cluster circuit using NAND gate
- The Decoder circuit designed utilizing body biasing circuit using NAND gate
- The Decoder circuit designed utilizing gate source biasing circuit using NAND gate

Simulation Results

The standard decoder modules are implemented on Cadence virtuoso using 20nm FinFET nodes. The corresponding results of the designs exhibited very good improvements compare to their counterparts and the sample transient response of the conventional 3 to 8 decoder is presented in Fig. 1.

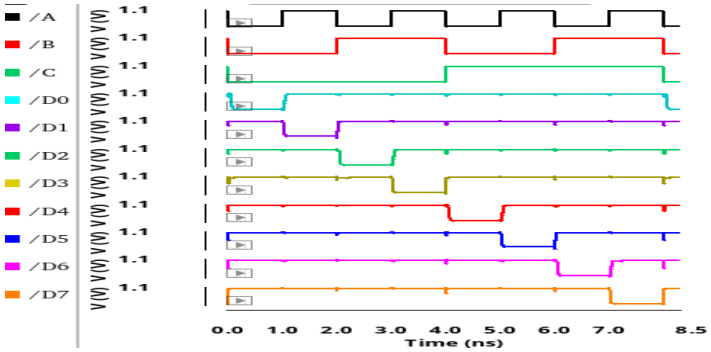

Fig. 8. Transient response of circuit shown in Fig. 1.

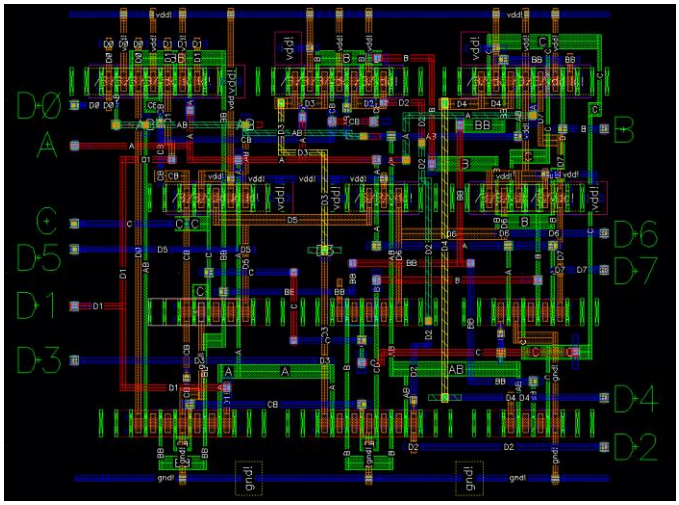

Fig. 9. Layout of circuit shown in Fig. 1.

The optimized area of the 3 to 8 decode is shown in Fig. 9 with the size of 8.74 μm^2.

Conclusion

In this proposed method the decoder circuit presented with two techniques that are cluster technique and source coupled technique. The FinFET has better control over channel (creation and construction/ group of objects), have better values of threshold, high electron ability to move around, current density, linearity and transconductance.

In different decoder design techniques, the cluster technique and source coupled technique are the better techniques for memory array application, where the source biasing decoder circuit configuration fulfills all the requirements. The circuit speed has been increased as compared to other techniques, this has less delay which is good for decoder designing in row and column. In the proposed Body biasing technique and clustering technique have four percentage improvements in dynamic power and Dynamic energy, twenty nine percentage improvements in delay calculation. There is an improvement of eleven percentages in static energy in the body biasing technique and leakage current.

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