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High Speed 3d DWT VlSI Architecture for Image Processing Using Lifting Based Wavelet Transform

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***Abstract*— Although the DCT-based image compression method using in the JPEG standard has been very successful in the several years, it still has some properties to improvement. A fundamental shift in the image compression approach came after the discrete wavelet transform (DWT) became popular, and it is adopted in the new JPEG 2000 standard So the digital information must be stored and retrieved in an efficient and effective manner, in order for it to be put to practical use. The Discrete Wavelet Transform (DWT) was based on time-scale representation. It provides efficient multi-resolution. DWT has been implemented by convolution method. For Such an implementation it requires a large number of computations and a large storage features that are not suitable for either high-speed or low-power applications. Hence the architecture for a high speed lifting based 3D (DWT) VLSI architecture is proposed. The lifting based DWT architecture has the advantage of lower computational complexities and also requires less memory. This lifting scheme has several advantages, including in-place computation of the DWT, integer-to-integer wavelet transform (IWT), symmetric forward and inverse transform. It uses a combination of 1D-DWT along with a set of memory buffers between the stages. The whole architecture was arranged in efficient way to speed up and achieve higher hardware utilization. It is desirable for high-speed VLSI applications.**

***Keywords*— Discrete Wavelet Transform, VLSI architecture, lifting, image compression, High-Speed.**

I. INTRODUCTION

The fundamental idea behind wavelets is to analyze according to scale. Indeed, some researchers in the wavelet field feel that, by using wavelets, one is adopting a perspective in processing data. Wavelets are functions that satisfy certain mathematical requirements and are used in representing data or other functions. This idea is not new. Approximation using superposition of functions has existed since the early 1800's, when Joseph Fourier discovered that he could superpose sines and cosines to represent other functions. However, in wavelet analysis, the scale that we use to look at data plays a special role. Wavelet algorithms process data at different scales or resolutions. FT with its fast algorithms (FFT) is an important tool for analysis and processing of many natural signals. FT has certain limitations to characterize many natural signals, which are non-stationary (e.g. speech). Though a time varying, overlapping window based FT namely STFT is well known for speech processing applications, a time-scale based Wavelet Transform is a powerful mathematical tool for non-stationary signals. Wavelet Transform uses a set of damped oscillating functions known as wavelet basis. WT in its continuous (analog) form is represented as CWT. CWT with various deterministic or non-deterministic basis is a more effective representation of signals for analysis as well as characterization. Continuous wavelet transform is powerful in singularity detection. A discrete and fast implementation of CWT is known as the standard DWT. With standard DWT, signal has a same data size in transform domain and therefore it is a non-redundant transform. A very important property was Multi-resolution Analysis allows DWT to view and process.

II. RELATED WORK

Wavelet transform has gained widespread acceptance in image compression research in particular. In addition, several VLSI architectures have been proposed for computing the 3D-DWT. They are mainly based on convolution scheme and lifting scheme**.** Dillen presented a combined architecture for the (5,3) and (9, 7) transforms with minimum area [5].Wang& Woon Seng Gan presented a folded architecture for lifting-based wavelet filters to compute the wavelet butterflies in different groups simultaneously at each decomposition level[6]. Wei Zhang etal. proposed the architecture in which it only requires minimum registers between the row and column filters as the transposing buffer, and a higher efficiency is achieved[7].

III. 3D-DWT

A. The Need For 3d DWT

Medical data needs a true 3-D transform for compression and transmission. DWT considers correlation of images, which translates to better compression. According to Lee, et al., the 3-D DCT is more efficient than the 2-D DCT for x-ray CT [1]. Likewise, one would expect the 3-D DWT to outperform the 2-D DWT for MRI. Wang and Huang showed the 3-D DWT to outperform the 2-D DWT by 40-90%[2] . The DWT has advantages over the DCT. First, DCT difference coding is computationally expensive. Second, wavelets do not cause blocking artifacts, which are unacceptable in medical images. The DCT is not best for medical image compression.

B. 3D-DWT

The 3-DWT is like a 1-D DWT in three directions. Refer to fig.1. First, the process transforms the data in the x-direction. Next, the low and high pass outputs both feed to other filter pairs, which transforms the data in the y-direction. These four output streams go to four more filter pairs, performing the final transform in the z-direction.

The process results in 8 data streams. The approximate signal, resulting from scaling operations only, goes to the next octave of the 3-D transform. It has roughly 90% of the total energy. Meanwhile, the 7 other streams contain the detail signals. Note that the conceptual drawing of the 3-D WT for one octave has 7 filter pairs, though this does not mean that the process needs 7 physical pairs. For example, a folded architecture maps multiple filters onto one filter pair.

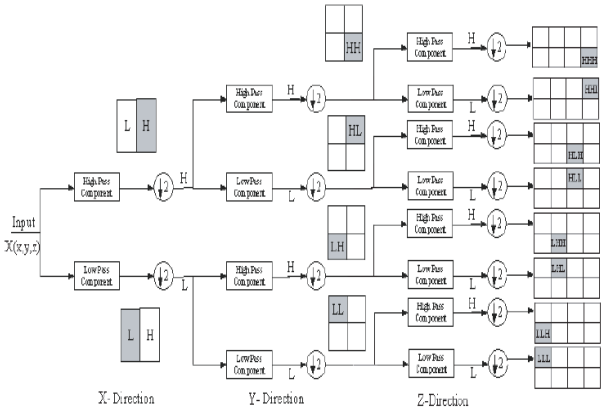

Figure 1: 3D-DWT in X ,Y and Z directions

C. Lifting Scheme

The basic idea behind the lifting scheme is very simple; try to use the correlation in the data to remove redundancy [3,4]. First split the data into two sets (split phase) i.e., odd samples and even samples as shown in Fig. 2. Because of the assumed smoothness of the data, we predict that the odd samples have a value that is closely related to their neighbouring even samples. We use *N* even samples to predict the value of a neighbouring odd value (predict phase). With a good prediction method, the chance is high that the original odd sample is in the same range as its prediction. We calculate the difference between the odd sample and its prediction and replace the odd sample with this difference. As long as the signal is highly correlated, the newly calculated odd samples will be on the average smaller than the original one and can be represented with fewer bits. The odd half of the signal is now transformed. To transform the other half, we will have to apply the predict step on the even half as well. Because the even half is merely a sub-sampled version of the original signal, it has lost some properties that we might want to preserve. In case of images we would like to keep the intensity (mean of the samples) constant throughout different levels. The third step (update phase) updates the even samples using the newly calculated odd samples such that the desired property is preserved. Now the circle is round and we can move to the next level. We apply these three steps repeatedly on the even samples and transform each time half of the even samples, until all samples are transformed.

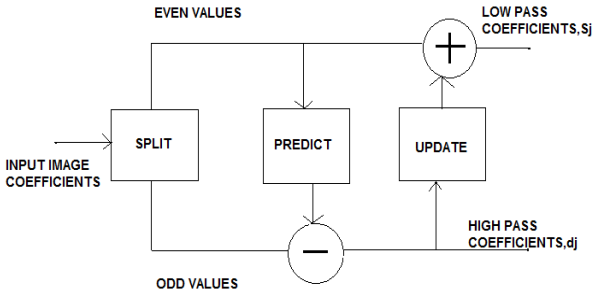

Figure 2: Block diagram of forward Lifting scheme

IV. 3D-DWT (9/7)

The (9/7) filter can be implemented by changing the coefficients ,it involves two stages (two predict and two update) as shown in Fig.3. The controller chooses the proper lifting coefficient for each clock cycle.

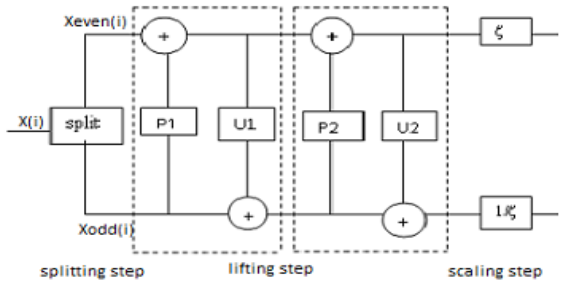

Figure 3: Architecture of 9/7 DWT based on lifting scheme

Basically 1-D (9, 7) DWT block diagram is developed based on the equations. The registers in the one half will operate in even clock where as the other half work in odd clock. The input pixels arrive serially row-wise at one pixel per clock cycle and it will get split into even and odd. So after the manipulation is done with the lifting coefficients 'a', 'b', 'c' and 'd' is done, the low pass and high pass coefficients will be given out. Hence for every pair of pixel values, high pass and low pass coefficients will be given as output respectively.

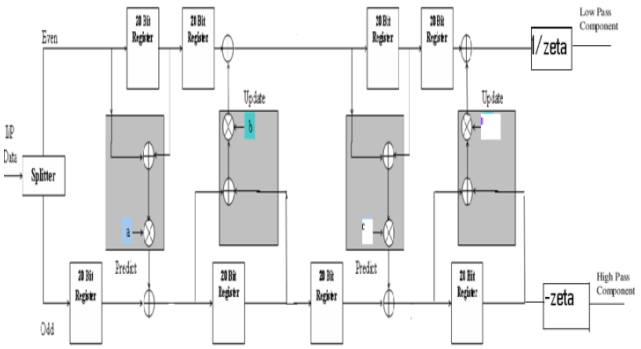

Figure.4: Computation of Basic (9,7) DWT Block in which 'coefficients 'a','b','c' and 'd' are lifting coefficients

V. RESULTS AND DISCUSSIONS

The test bench is developed in order to test the modeled design. This developed test bench will automatically force the inputs and will make the operations of algorithm to perform.

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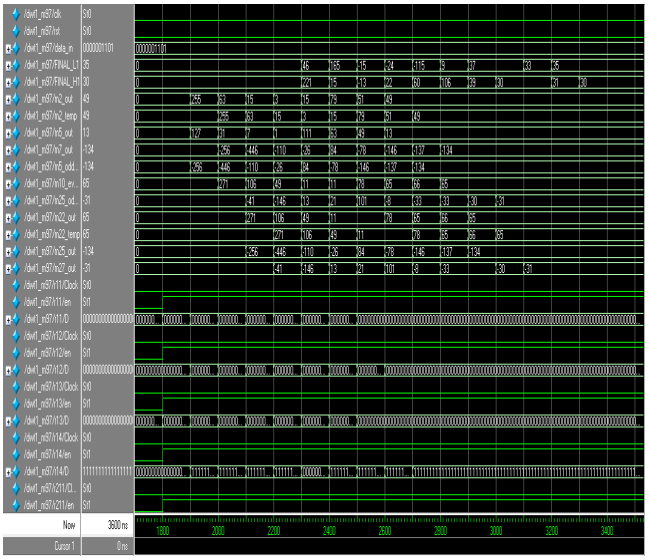

Figure 5: Simulation Result of DWT(9/7) Block with High and Low Pass Coefficients

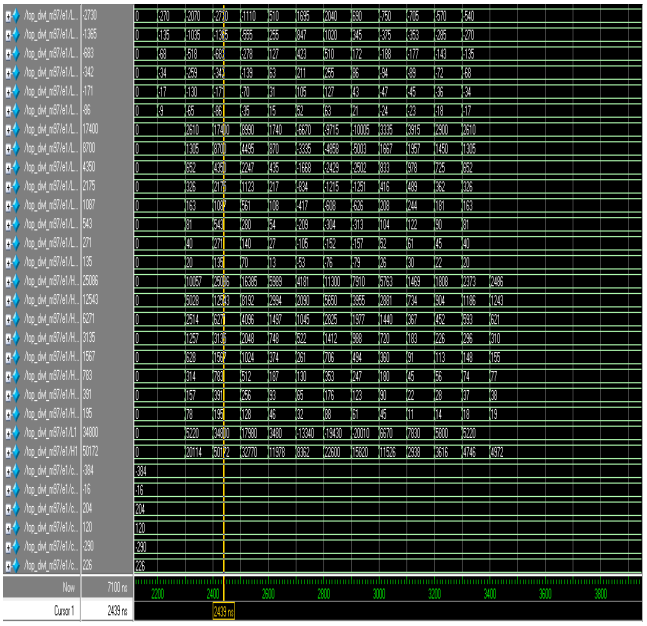

Figure 6: Simulation Result of 3D-DWT(TOP MODULE) Block with High and Low Pass Coefficients

Since the operation of this DWT block has been discussed in the previous chapter, here the snapshots of the simulation results were directly taken in to consideration and discussed. For this DWT block, the clock and reset were the significant inputs. The pixel values of the image, that is, the input data will be given to dwt block and hence these values will be split in to even and odd pixel values. In the design, this even and odd were taken as a array which

will store its pixel values in it and once all the input pixel values over, then load will be made high which represents that the system is ready for the further process.

The input is 16 bits each input bit width is vary because of the multiplier. The DWT consists of registers,multipliers and adders. Once the input is send, the data is divided into even data and odd data. The even data and odd data is stored in the temporary registers. When the reset is high the temporary register value consists of zero when ever the reset is low the input data split into the even data and odd data. The input data read up to sixteen clock cycles after that the data read according to the lifting scheme. The output data consists of low pass and high pass elements
This is the 1-D discrete wavelet transform as shown in fig.5. The 2-D discrete wavelet transform is that the low pass and the high pass again divided into LL, LH and HH, HL. The 3-D discrete wavelet transform is that the low pass and the high pass again divided into LLL, LLH, LHL, LHH, HLL, HLH, HHL, and HHH. The output is verified in the ModelSim.

SYNTHESIS REPORT:
---- Source Parameters
Input File Name : "Top_dwt_m97.prj"
Input Format : mixed
Ignore Synthesis Constraint File : NO
---- Target Parameters
Output File Name : "Top_dwt_m97"
Output Format : NGC
Target Device : xc3s100e-5-vq100
Optimization Goal : Speed
Optimization Effort : 1
RAMs : 14
10x120-bit dual-port distributed RAM :8
12x60-bit dual-port block RAM :2
12x60-bit dual-port distributed RAM :2
8x10-bit dual-port distributed RAM :2
Multipliers : 42
200x10-bit registered multiplier : 42
Adders/Subtractors : 56
200-bit adder : 56
Counters : 14
4-bit up counter : 14
Registers : 10367
Flip-Flops : 10367
Comparators : 21
4-bit comparator greater : 7
4-bit comparator lessequal : 14

DWT-1 BLOCK:

Final Results
RTL Top Level Output File Name : dwt1_m97.ngr
Top Level Output File Name : dwt1_m97
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : NO Design Statistics
IOs : 134
Cell Usage :
BELS : 9449
GND : 1
INV : 603
LUT1 : 89
LUT2 : 2536
LUT3 : 15
LUT4 : 5
MUXCY : 3384
VCC : 1
XORCY : 2815
FlipFlops/Latches : 790
FDR : 759
FDRE : 29
FDSE : 1
FDSE_1 : 1
RAMS : 20
RAM16X1D : 20
Clock Buffers : 1
BUFGP : 1
IO Buffers : 133
IBUF : 11
OBUF : 122

Device utilization summary:

Selected Device : 3s100evq100-5
Number of Slices : 2055 out of 960 214%
Number of Slice Flip Flops: 790 out of 1920 41%
Number of 4 input LUTs: 3288 out of 1920 171%

Number used as logic: 3248
Number used as RAMs: 40
Number of IOs: 134
Number of bonded IOBs: 134 out of 66 203%
Number of GCLKs: 1 out of 24 4%

Timing Summary:

Speed Grade: -5
Minimum period: 22.555ns (Maximum Frequency: 44.335MHz)
Minimum input arrival time before clock: 4.112ns
Maximum output required time after clock: 4.380ns
Maximum combinational path delay: No path found

VI. CONCLUSION

The architecture is developed for lossy compression, which is based on the lifting algorithm of Daubechies (9,7) filters. This work ensures that the image pixel values given to the DWT process which gives the high pass and low pass coefficients of the input image. The simulation results of DWT were verified with the appropriate test cases using ModelSim and synthesis report generated using Xilinx. The advantages of the proposed architecture are fast computing time and control complexity will be low. In Future, this Architecture could be implemented in FPGA. It will be also possible to provide multilevel decomposition for 3D-DWT.

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