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Research Article

State of art design of novel adder modules for future computing

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ABSTRACT
This paper presents power analysis of the seven full adder cells reported as having a low PDP (Power Delay Product), by means of speed, power consumption and area. These full adders were designed upon various logic styles to derive the sum and carry outputs. All these full adders designed using TDK 90 nm Technology and simulated using mentor graphics EDA tool with BSIMv3 (model 49). And the layouts of all these full adders designed in Icstation of Mentor Graphics.

Keywords: Adders, pass logic implementations, logic devices, low- power, power delay product, layout design.

1. Introduction

In portable electronic devices, it is important to prolong the battery life as much as possible. Adder is the core component of an arithmetic unit. The efficiency of the adder determines the efficiency of the arithmetic unit. Various structures have evolved trying to improve the performance of the adder in terms of area, power and speed. Low power design with high speed of operation is more essential [1]-[12].

The fundamental arithmetic operation is Addition and it is used extensively in many VLSI systems such as application-specific DSP architectures and microprocessors. in addition to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation, etc. in most of these systems the adder is part of the critical path that determines the overall performance of the system [13]-[25].

The amount of energy spent during the realization of a determined task relates to PDP and stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies. The PDP exhibited by the full-adder would affect the system's overall performance [26]-[33].

The new full adder cell designed using an alternative logic structure that is based on the multiplexing of the Boolean functions XOR/XNOR and AND/OR, to obtain the SUM and CARRY outputs, respectively. These full adders show to be more efficient on regards of power consumption and PDP when compared with other ones reported previously as good candidates to build low-power arithmetic modules [34]-[36].

2. Conventional Full Adder Designs

Transmission function theory was used to build a full adder formed by three main logic blocks: a XOR-XNOR gate to obtain A $\oplus$ B and A $\odot$ B signals (Block 1), and XOR blocks or multiplexers to obtain the SUM (So) and CARRY (Co) outputs (Blocks 2 and 3), as shown in Figure 1 [37]-[40].

This logic structure is based on the full adder's true-table shown in Table I, and it has been adopted as the standard internal configuration in most of the enhancements developed for the 1-bit full adder cell. After a deep comparative study, the most efficient realization for block I was extracted: the one implemented with SR-CPL logic style. But another important conclusion has pointed out over there: the major problem on regards of propagation delay for a full adder built upon the logic structure shown in Figure 1 is that it is necessary to obtain the A $\oplus$ B and A $\odot$ B intermediate signals, which are then used to drive other blocks in order to generate the final outputs. Thus, the overall propagation delay and, in most of the cases, the power consumption of the full adder, depend on the delay and voltage swing of the A $\oplus$ B and A $\odot$ B signals, generated within the cell [41]-[44].

Therefore, to increase the operational speed of the full adder, it is necessary to look out for a new logic structure that avoids the generation of intermediate signals used to control the selection or transmission of other signals located on the critical path.

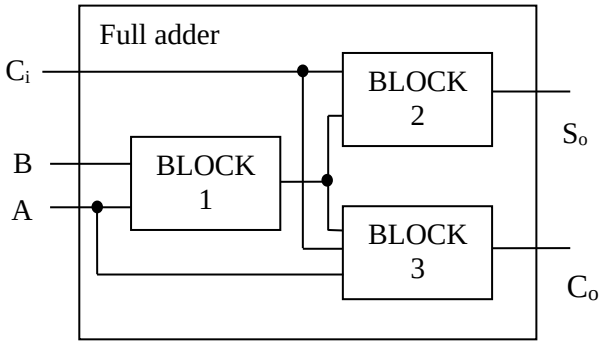

Fig.1. Full-adder cell formed by three main logical blocks.

2.1. HPSC Full Adder

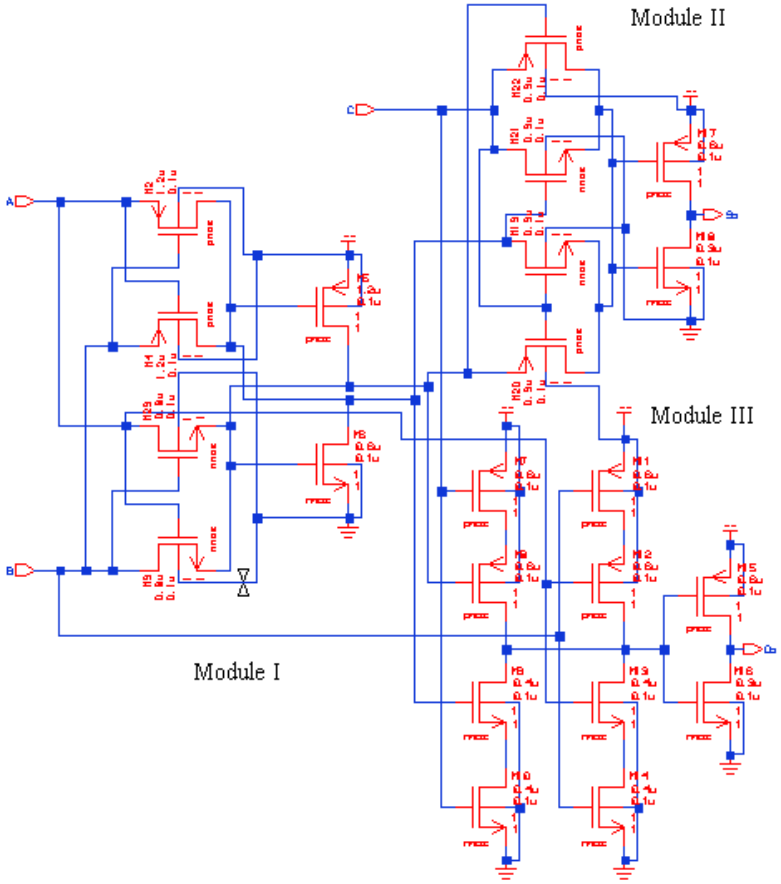

Fig.2. Schematic diagram of the HPSC full adder.

The simultaneous generation of XOR and XNOR outputs by pass logic is advantageously exploited to a novel complementary CMOS stage to produce full-swing and balanced outputs so that adder cells can be cascaded without buffer insertion. The increase in transistor count of the complementary CMOS stage is compensated by its reduction in layout complexity.

As pass transistor logic has been known to implement XOR function more efficiently than the complementary CMOS, Module I and Module II are implemented using pass-transistor logic. For Module III, a novel circuit structure is created which gives rise to the performance gain over those circuits to be compared. The two complementary feedback transistors restore the weak logic caused by pass transistors. They restore the non full-swing output by either pulling it up through PMOS to the power supply or down through NMOS to ground so that sufficient drive is provided to the successive modules. In addition, since there is no direct path between power-supply and ground, short circuit current has been eliminated. There are several choices for Module II. Since its logic expression is similar to that of Module I, the cross-back 6- transistor circuit can also be used. However, it has insufficient driving power due to the lack of input-output decoupling. Therefore, we use a similar circuit as that of TFA, but fully exploit the available XOR and XNOR outputs from

Module I to allow a single inverter to be attached at the last stage. The output inverter guarantees sufficient drive to the cascaded cell.

$$\overline{C_{out}} = \overline{AB + C_{in}(A \oplus B)}$$

This circuit has inherited the advantages of complementary CMOS, which has been proven in to be superior in performance to all pass transistor logic styles for all logic gates except XOR at high supply voltage. Its robustness against voltage scaling and transistor sizing (high noise margins) enables it to operate reliably at low voltages and arbitrary (even minimal) transistor sizes.

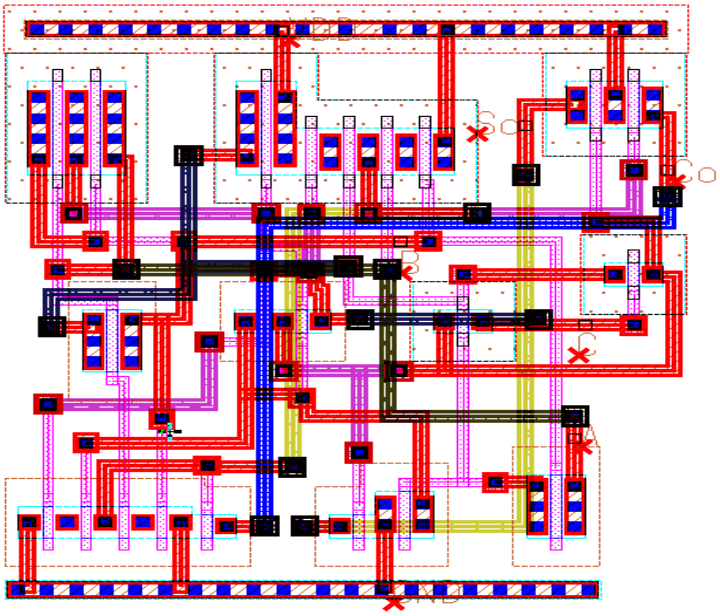

Fig 3. Layout of the HPSC full-adder.

2.2. Hybrid Full adder

The sum and carry generation circuits of the proposed full adder are designed with hybrid logic styles. To operate at ultra-low supply voltage, the pass logic circuit that co generates the intermediate XOR and XNOR outputs have been improved to overcome the switching delay problem. The increase in the transistor count of its complementary CMOS output stage is compensated by its area efficient layout.

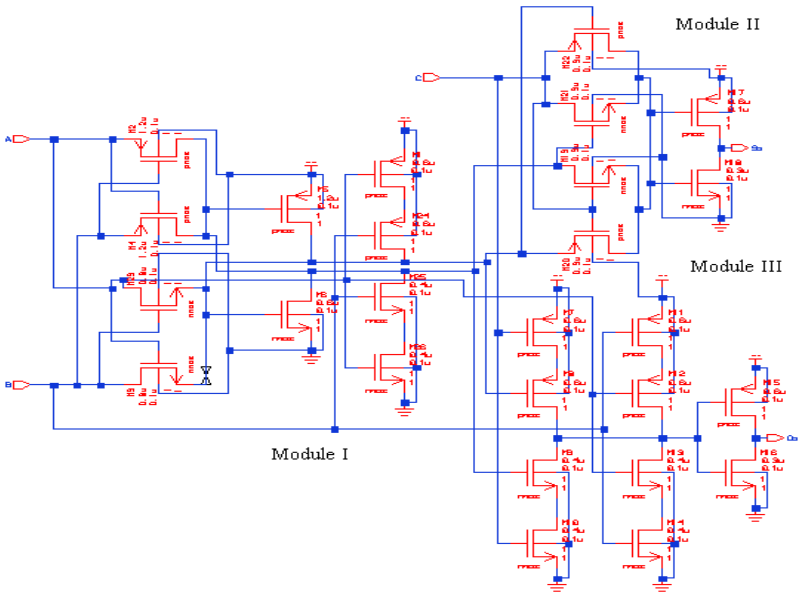

Fig.4. Schematic diagram of the HYBRID full adder

As shown in Fig. 4, the proposed hybrid full adder circuit can be decomposed and analyzed in three sub modules. The logic expressions for the intermediate signals and outputs are given as follows:

$$Y = A \oplus B$$

$$Y' = \overline{A \oplus B}$$

$$Sum = Y \oplus Cin$$

$$Cout = A \cdot B + C_{in} \cdot Y$$

One approach to realize the exclusive OR and exclusive NOR (XOR/XNOR) functions is to synthesize the XOR function and generate the XNOR function through an inverter (e.g., TFA and TGA). This type of design has the disadvantage of delaying one of the Y and Y' outputs, giving rise to skewed signal arrival time to the successive modules. This will increase the chance of producing spurious switching and glitches in the last two modules. A better approach is to use different sets of transistors to generate the XOR and XNOR functions separately, with the possibility of introducing a larger transistor count. To reduce the number of transistors, a pass transistor circuit with only six transistors is used to generate the balanced XOR and XNOR functions. Comparing with those designs that use an inverter to generate the complement signal, the switching speed is increased by eliminating the inverter from the critical path. The two complementary feedback transistors restore the weak logic caused by the pass transistors. They restore the non full-swing output by either pulling it up through pMOS to the power supply or down through nMOS to ground so that sufficient drive is provided to the successive modules. In addition, since there is no direct path between the power supply and ground, short-circuit current has been reduced.

There are several choices for Module 2. Since its logic expression is similar to that of Module I, the cross back 6-transistor circuit can also be used. However, it suffers from insufficient driving power due to the pass transistors. Therefore, a similar circuit as that of TFA and 14 T used, but fully exploit the available XOR and XNOR outputs from Module I to allow only a single inverter to be attached at the last stage.

The smallest number of transistors for generating the Cout signal is two, but it suffers from the threshold voltage drop problem. Although a 4-transistor circuit can be used to generate a full swing signal, it does not provide enough driving power. This can be proven in the later section when it is compared with our proposed circuit. The new circuit is based on complementary CMOS logic style, its logic expression is given by

$$C_{out} = A \bullet B + C(A \oplus B)$$

This circuit has inherited the advantages of complementary CMOS logic style, which has been proven to be superior in performance to all pass transistor logic styles for all logic gates except XOR at high supply voltage. Its robustness against voltage scaling and transistor sizing (high-noise margins) enables it to operate reliably at low voltage and arbitrary (even minimal) transistor size.

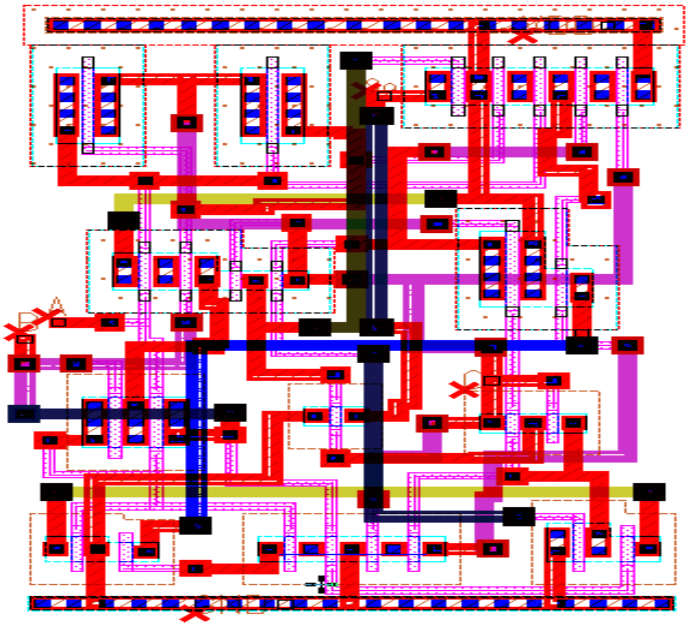

Fig 5. Layout of the HYBRID full-adder.

2.3. Hybrid CMOS Full adder

This full adder is based on a novel XOR–XNOR circuit that generates XOR and XNOR full-swing outputs simultaneously. This output stage provides good driving capability enabling cascading of adders without the need of buffer insertion between cascaded stages. This full adder is energy efficient and outperforms several standard full adders without trading off driving capability and reliability. The new full-adder circuit successfully operates at low voltages with excellent signal integrity and driving capability.

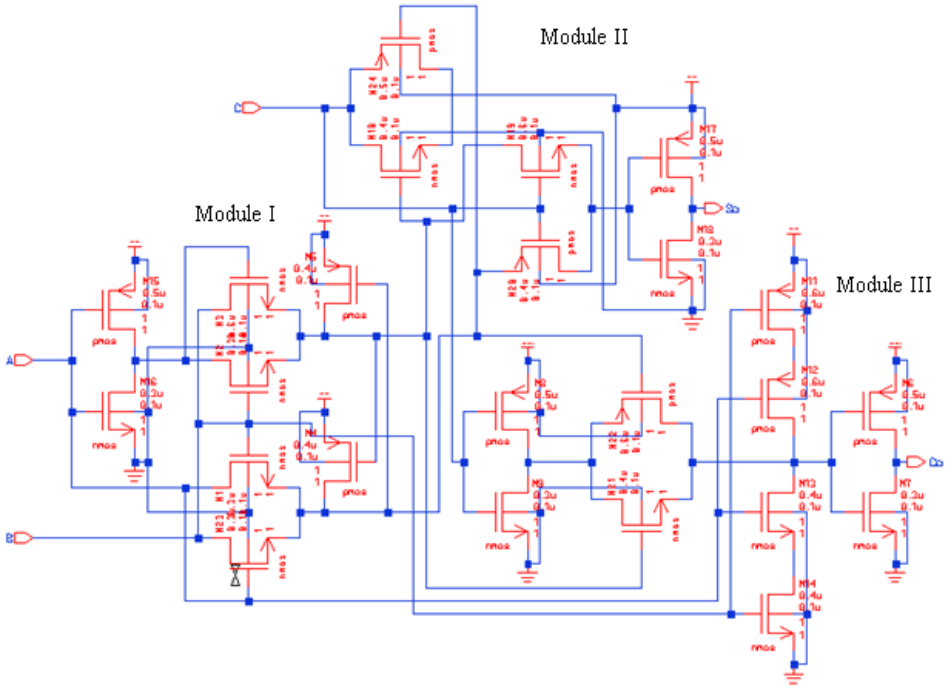

Fig 6. Schematic diagram of the HYBRID CMOS full adder

The centralized full adders, both XOR and XNOR circuits are present (both in module I) that generate the intermediate signals H and H'. These signals are passed on to module II and III along with the carry from the previous stage and the other inputs A and B to produce the Sum and Cout. For the new adder, two proposed circuits and one existing circuit in the three modules has used. The proposed adder is shown in Fig. 7.4.

In module I, the proposed XOR–XNOR circuit produces balanced full-swing outputs. It has high-speed operation due to the cross-coupled pMOS pull-up transistors providing the intermediate signals quickly. Since the other two modules rely heavily on the intermediate signal H and H' to produce the final outputs, the delay response of module I is critical. The proposed XOR–XNOR circuit is 1.7 faster than the best available XOR–XNOR circuits. Due to this reason, the new adder is faster than the compared adders.

Module II is a transmission-function implementation of XNOR function to generate the followed by an inverter to generate. This provides good driving capability to the circuit. Due to the absence of supply rails there are no short circuit currents. The circuit is free from the problem of threshold loss and has the lowest PDP amongst all circuits that are used for module II.

Module III employs the proposed hybrid-CMOS output stage with a static inverter at the output. This circuit has a lower PDP as compared to the other existing designs. The static inverter provides good driving capabilities as the inputs are decoupled from the output. The structure of the circuit is very symmetric and, therefore, the layout is regular. Due to the low PDP of module II and module III, the new adder is expected to have low power consumption.

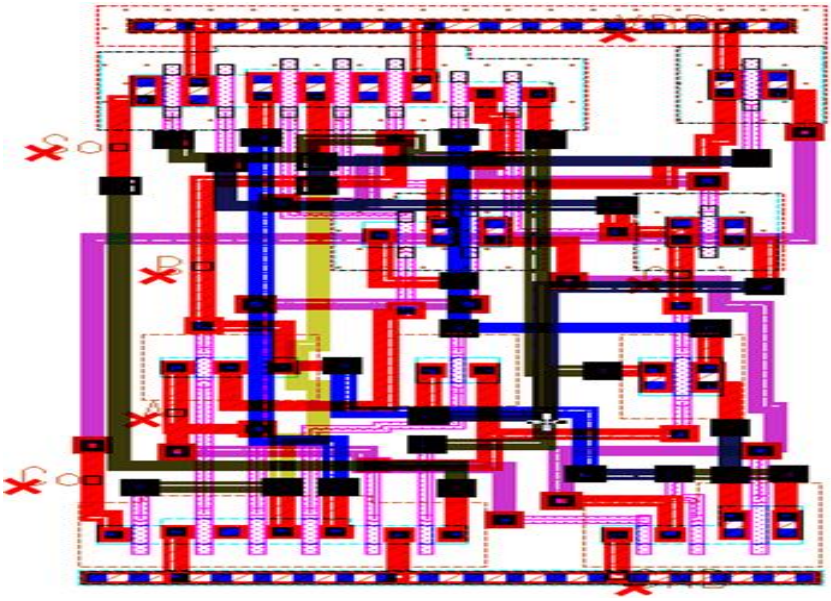

Fig 7. Layout of the HYBRID CMOS full-adder.

2.4. CPL Full adder

The main concept behind the CPL is the use of an NMOS pass transistor network for logic realization and elimination of the PMOS transistor. CPL consists of complementary inputs/outputs, an NMOS logic network and CMOS output inverters as shown in fig.8. Due to positive feedback and use of NMOS transistors, the circuit is inherently fast. This property is utilized to reduce the width of the transistors to reduce power consumption without much speed degradation. The proposed adder has a balanced structure with respect to generation of 'sum' and 'carryout' signals.

The number of transistors used in this design is more compared to other designs. This is due requirement of seven inverters to generate complement signals. However, when this adder is used in designs such as the multiplier, the input complementary signals can be derived from previous stage outputs. This reduces the number of transistors. Also, the drivability of this adder is fairly good even without the use of inverters. This is due to use of pull-up PMOS transistors. Hence, the output inverters can be used in alternate stages of the design. Similarly, in complex designs like the multiplier, the output inverters for generating sum and carry can be used in alternative stages, thereby improving speed and reducing area.

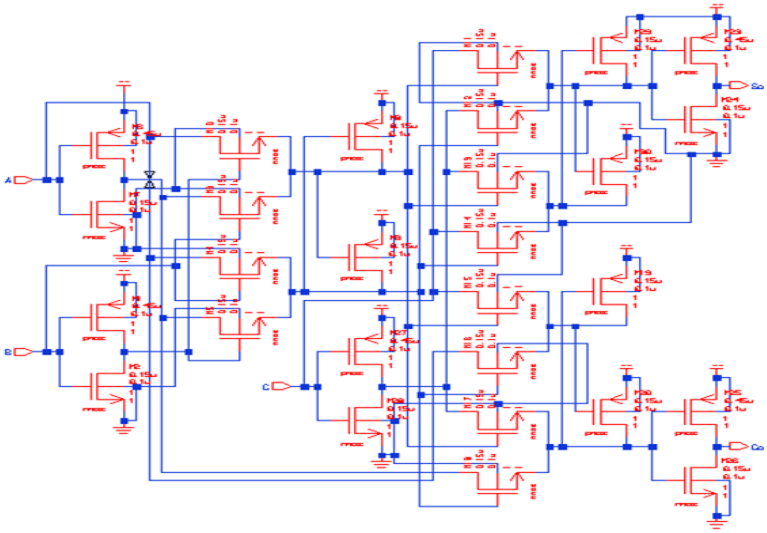

Fig.8. Schematic diagram of the CPL full adder.

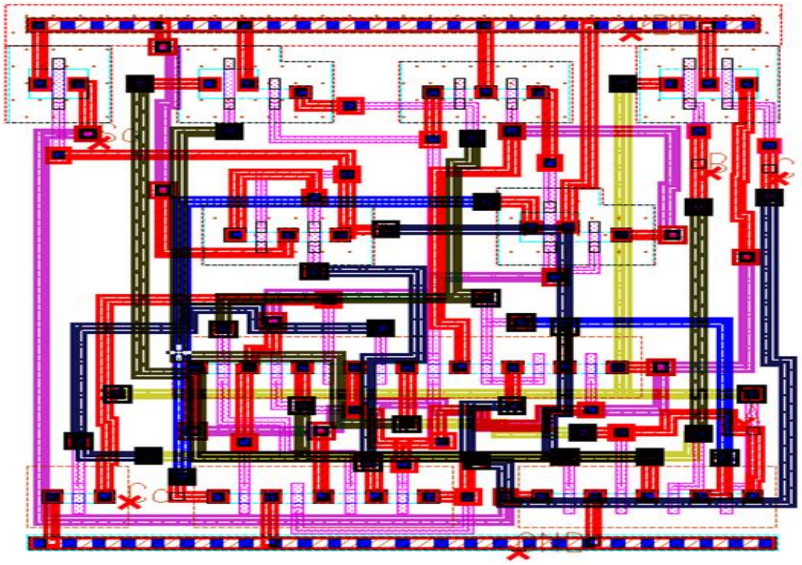

Fig.9. Layout of the CPL full-adder.

2.5. New14t Full adder

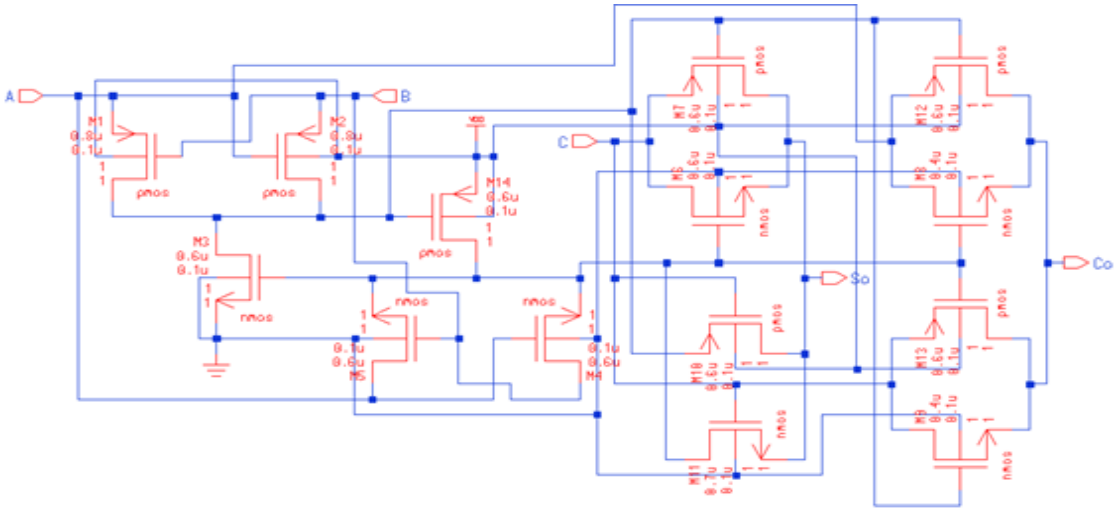

Fig.10. Schematic diagram of the new14T full adder

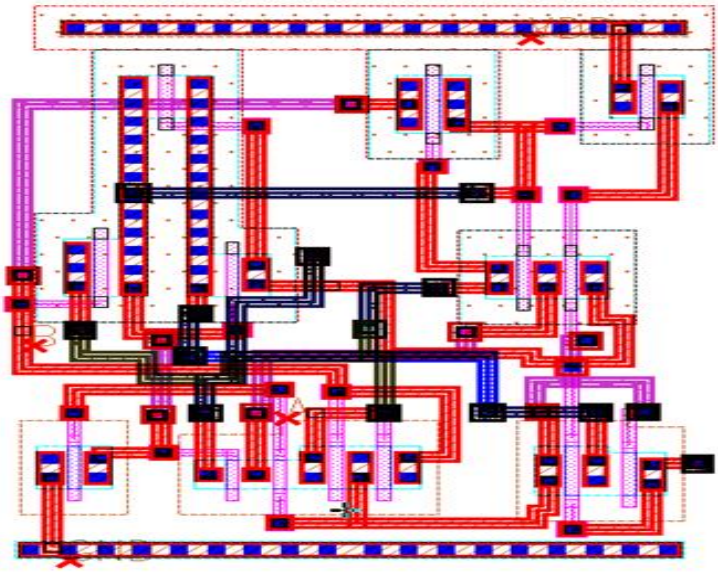

Fig.11. Layout of the NEW14T full-adder.

This new cell can reliably operate within certain bounds when the power supply voltage is scaled down, as long as due consideration is given to the sizing of the MOS transistors during the initial design step. A low transistor count full adder cell using the new XOR-XNOR cell is also presented.

From gate logic design experience, it is well known that a full adder can be best implemented using exclusive-OR (XOR) gates, since the 'sum' can be expressed as an XOR function of all its inputs and the 'carry' as a multiplexer function controlled by the XOR function. A pass transistor is an nMOS (pMOS) transistor with the signal input fed to the source and the signal output taken from drain. A pass network is an interconnection of a number of pass transistors to achieve a particular switching function. The propagation of the signal through the transistor is controlled by a signal applied to its gate. In the case of an nMOS transistor, a logic '1' at the gate passes the input from source to drain and a logic '0' opens the source to drain path. A PMOS transistor exhibits similar behaviour with a control signal of logic level 0.

3. Alternative Logic Structure For A Full Adder

Examining the full-adder's true-table in Table I, it can be seen that the So output is equal to the AB value when C=0, and it is equal to A+B when C=1. Thus, a multiplexer can be used to obtain the respective value taking the C input as the selection signal. Following the same criteria, the Co output is equal to the A · B value when C = 0, and it is equal to A + B value when C = 1.

Table I: True-Table for A 1-Bit Full-Adder: A, B, and C Are Inputs; So And Co Are Outputs

C	B	A	So	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Again, C can be used to select the respective value for the required condition, driving a multiplexer. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the A B and A B signals, another block to obtain the A · B and A + B signals, and two multiplexers being driven by the C input to generate the So and Co outputs, as shown in Fig. 12 .

The features and advantages of this logic structure are as follows.

• There are not signals generated internally that control the selection of the output multiplexers. Instead, the C input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.

• The capacitive load for the C input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the C signal falls on the critical path can be reduced.

• The propagation delay for the So and Co outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation (e.g., wave pipelining), and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.

• The inclusion of buffers at the full-adder outputs can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NOR gates at the input of the multiplexers, improving in this way the performance for load-sensitive applications.

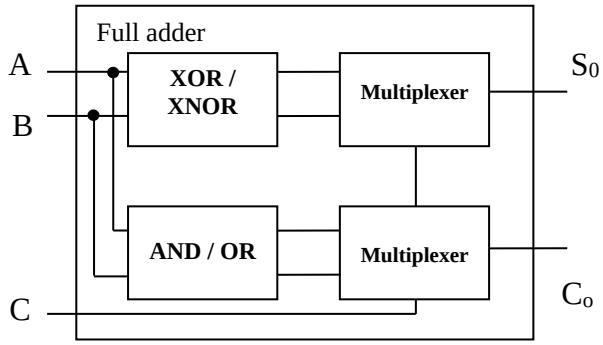

Fig.12. Alternative logic scheme for designing full-adder cells.

3.1. DPL Full adder

Two new full-adders have been designed using the logic styles DPL and SR-CPL, and the new logic structure presented in Fig. 13. Fig. 15 presents a full-adder designed using a DPL logic style to build the XOR/XNOR gates, and a pass-transistor based multiplexer to obtain the So output. In Fig. 4, the SR-CPL logic style was used to build these XOR/XNOR gates. In both cases, the AND/OR gates have been built using a powerless and groundless pass-transistor configuration, respectively, and a pass-transistor based multiplexer to get the Co output.

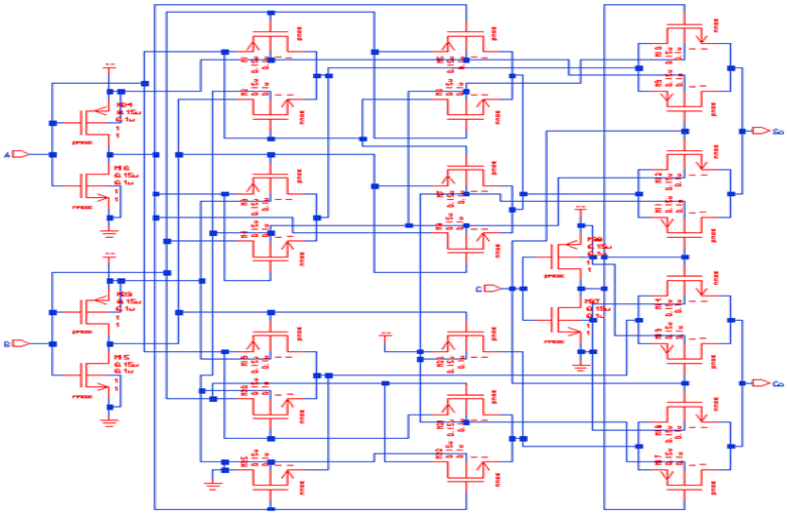

Fig.13. Full-adder designed with a DPL logic style.

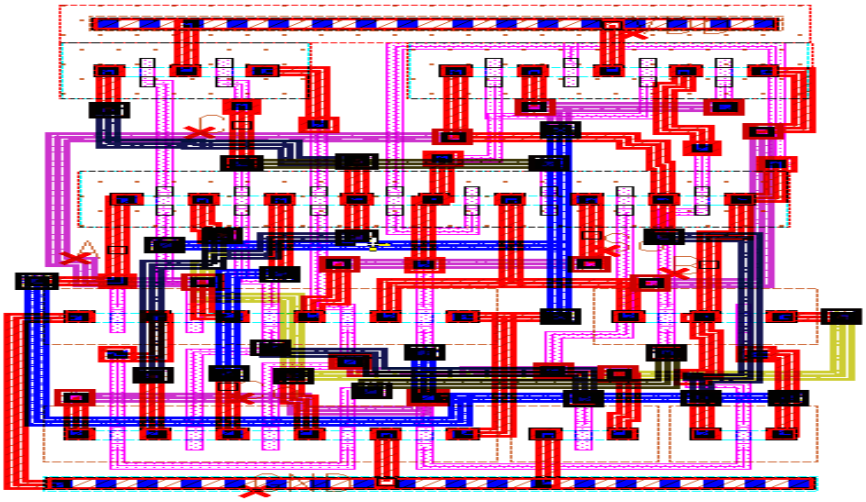

Fig.14. Layout of the DPL full-adder.

3.2. SRCPL Full adder

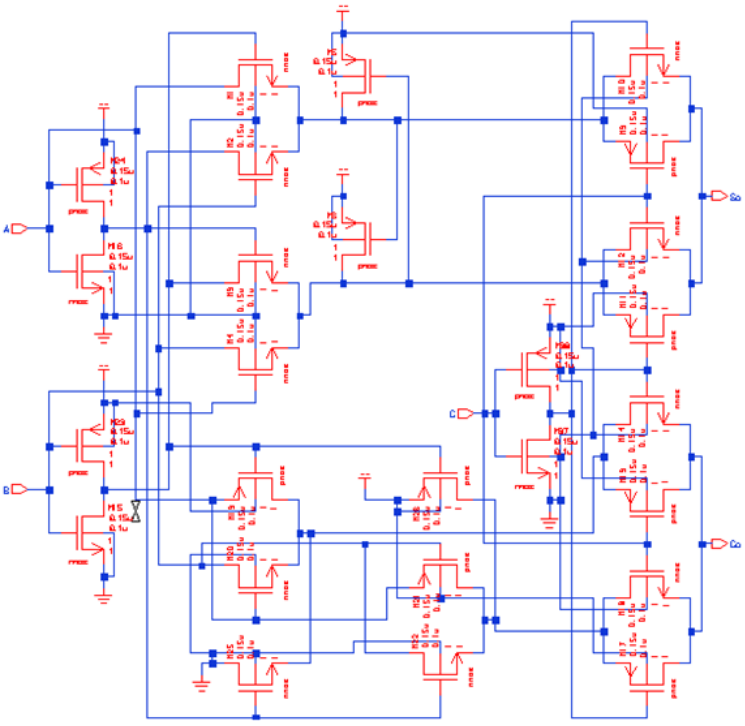

Fig.15. Full-adder designed with the SR-CPL logic style.

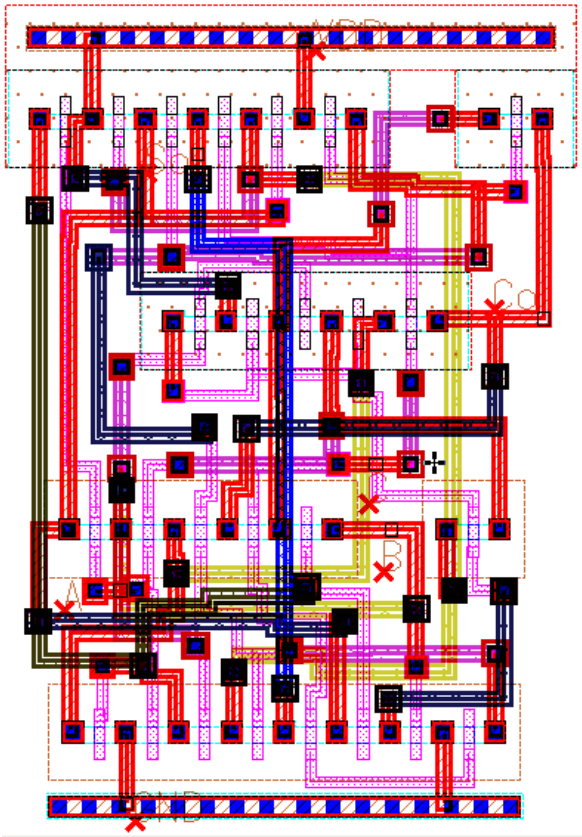

Fig.16. Layout of the SRCPL full-adder.

4. Simulation Setup

The test bed used to simulate the full adders being compared is shown in Figure 5. This simulation environment has been commonly used to compare the performance of the full adders. The advantage of using this test bed is that the Following power components are taken into account, besides the dynamic one:

The short-circuit dissipation of the inverters connected at the full adder inputs.

- This power consumption varies according to the capacitive load that the adder module offers at the inputs. Even more, the energy required to charge and discharge the full adder internal nodes when the module has no direct power supply connections (such is the case of pass-transistor logic styles), comes through these inverters connected at the full adder inputs.
- The short-circuit consumption of the full adder itself, as it is receiving signals with finite slopes coming from the buffers connected at the inputs, instead of ideal ones coming from voltage sources.
- The short-circuit and static dissipation of the inverters connected to the outputs of the full adder due to the finite slopes and degraded voltage swing of the full adder output signals.

The importance of including the effects and power consumption of the buffers connected at the inputs and outputs of the full adder cell come from the fact that the module is always going to be used in combination with other modules to build a larger system, and these static inverters are a good generalization for any other module to be considered.

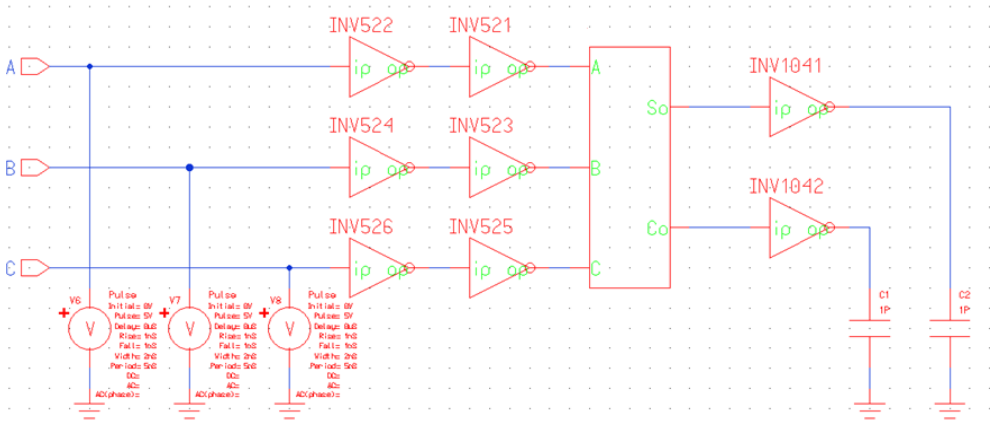

Fig.17. Test bed used for simulating the full-adders under comparison.

5. Simulation Results

Seven full adders were compared on regards of power consumption and delay. They were named: new14T[1], HPSC[2], HYBRID[3], HYBRID CMOS[4], CPL[5], DPL and SR-CPL[6].

The schematics and layouts were designed using a TDK 90 nm CMOS technology, and simulated using the BSIM3v3 model (level 49) and the post-layout extracted netlists containing R and C parasitics. Simulations were carried out using ICSTUDIO in Mentor Graphics Eda Tool. Table 2 shows the simulation results for full-adders performance comparison, regarding power consumption, propagation delay, PDP and area.

The ICSTUDIO in Mentor Graphics EDA Tool simulations showed that of 59.56% power savings and 57.51% for the PDP for the joint optimization at 5v. And 52.32% power savings and 48.83% for the PDP for the joint optimization at 1.8v.

6. Conclusion

The design of high-speed low-power full adder cells based upon an alternative logic approach has been presented. MENTOR GRAPHICS EDA TOOL simulations have shown a great improvement on regards of power-delay metric for the proposed adders, when compared with previously published realizations designed with TDK 90 nm technology.

The full adders designed upon this logic structure and DPL and SR-CPL logic styles, exhibit a delay around 134.9 ps and power consumption around 4.22 μW at 1.8v and the delay is around 171.7 and power dissipation is 491.1 μW at 5v supply voltage, for an overall reduction of 81% respect to the best featured one of the other adders been compared, but in general about 50% respect to the other ones.

Some work can be done in the future on the design of 45 nm technology of high-speed low-power full adders.

Table III: Simulation Results of the Full-Adders Compared

S.No.	Name of the full adder	No. of transistors	Frequency	Area (μm2)		
				L	W	L*W
1	NEW14T	14	200 MHZ	5.14	7.75	39.83
2	HYBRID CMOS	24	200 MHZ	4.92	9.07	44.61
3	HPSC	22	200 MHZ	6.49	7.60	49.31
4	HYBRID	26	200 MHZ	5.76	9.57	55.11
5	CPL	28	200 MHZ	7.37	8.29	61.10
6	DPL	28	200 MHZ	4.89	7.95	38.87
7	SRCPL	26	200 MHZ	5.40	7.72	41.69

S.No.	Name of the full adder	at 5v Supply voltage				
		Power dissipation(uW)	Propagation delay (ps)			PDP (uw*ps)
			Sum	Carry	Average delay	
1	HYBRID	1206.5	147.1	160.59	153.8	185668.28
2	HPSC	1214.6	146.6	152.19	149.3	181455.16
3	HYBRID CMOS	912.2	205.4	171.19	188.3	171815.14
4	NEW14T	983.8	152.3	146.70	149.5	147081.88
5	CPL	540.3	205.7	204.79	205.2	110931.59
6	DPL	491.3	189.1	176.56	182.8	89837.66
7	SRCPL	490.9	139.9	181.49	160.6	78893.24

S.No.	Name of the full adder	at 1.8v Supply voltage				
		Power dissipation (uW)	Propagation delay (ps)			PDP (uw*ps)
			Sum	Carry	Average delay	
1	NEW14T	8.85	136.1	115.4	125.8	1113.33
2	HYBRID CMOS	6.13	153.9	131.8	142.9	876.65
3	HYBRID	6.57	108.3	133.3	120.8	793.54
4	HPSC	6.57	108.2	125.0	116.6	765.83
5	CPL	4.65	142.6	147.1	144.8	673.27
6	DPL	4.23	133.6	158.8	146.2	617.93
7	SRCPL	4.21	98.8	148.7	123.6	521.23

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