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Research Article

Analog to digital converter: Novel Methodology

NIDHAL ABDULAZIZ[1], S. AMIN[2], M. BILAL[3]
[1,2,3]School of Computer Science, National College of Business Administration and Economics, Lahore 54660, Pakistan
Email: Nid.abd@ncbae.edu.pk[1], amin.s@ncbae.edu.pk[2], m.bilal@ncbae.edu.pk[3]
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ABSTRACT
nowadays, the modern microelectronics digital communication systems are using low power and efficient design for wide variety of applications in real world. Recent researchers focusing on amplifier circuits for increasing applications with novel designs; conventional method uses FinFET CMOS design, and other reconfigurable designs, which consumes much power on designing and to overcome the design complexity of existing work, the proposed optimal power reduction strategy is employed on the ADC lock-in amplifier. Here the two stage lock-in amplifier is constructed with gated clocking of DFF switching strategy to reduce the power consumption and to obtain better results than previous works. Virtext FPGA model of amplifier is designed with Xilinx ISE 14.2 tool. The design of lock-in Amplifier has both sensing stage and latch stage with better sampling periods of edge triggering state, which improves the performance. High speed FPGA with mixed signal processing application is capable for this design. Experimental results analyzed with the power, area and delay as major concern and switching state with clocking model determines the high speed design. By comparing with the previous work, the proposed work is designed to achieve better results.

Keywords: ADC; FPGA Virtex and gated clock; Lock-in Amplifier; Power reduction approach.

Introduction

Recent communication and measuring framework plans are expanding in intricacy as the most recent elite processors and DSPs empower new sign preparing methods. As framework prerequisites for speed and goal increment, more fit Analog-to-Digital Converters (ADCs) arise, and thus require better Analog Front Ends. Lock-in amplifier have been broadly utilized for estimating powerless signs in various fields, for example, Raman spectroscopy, nuclear power microscopy, multifunctional examining burrowing microscopy and sensors [1]. The estimation rule has a correlative demodulation with a similar frequency as the transporter sign to single out the segment of the sign at a particular reference of frequency and phase. Advanced lock-in amplifiers could be utilized in impedance estimation, which has at any point been executed by complementary metal oxide semiconductor (CMOS) innovation [2]. The electrical impedance spectroscopy (EIS) framework dependent on CMOS innovation, which had a 1mHz to 100 kHz recurrence range with a 2.65% average error [1]-[14]. Analog to digital converter circuit utilizes the sampling rate to trigger the digitalized converter. Nyquist sampling rate determines the sampling theorem of amplifier [3]. DSP scheme mimics a zero-intermediate-frequency analog down converter as found in Signal frequency designs, but this is not the only available approach [4]. Complex fast Fourier transforms (FFTs) can be performed on the digitized signals that will yield similar and possibly more useful results [5]. A Bipolar input is significant on the grounds that at exceptionally low frequencies; here the AC coupling capacitors get tremendous and bipolar information can wipe out the coupling capacitor in low frequency tests [6]. The ADC information is put away straightforwardly in the processors with RAM disposing of the requirement for an outer FPGA and memory. The operation amps utilized are blend of Linear Technology, Burr-Brown and Analog Devices. Superior operation amps are a workmanship and here is one market that isn't so commoditized [7]. Every producer has one specialty that they dominate in, subsequently you need to purchase from all to get the best exhibition. LIA duplicates the sign with an unadulterated sine wave, gauges the single Fourier segment of the sign at the reference frequency [8].

Signal processing in device implementation consistently be sought after investigations endeavor to weak signal for getting better performance analysis [15]-[25]. For expanding the signal to extracted proportion of a boisterous sign, the most helpful exploratory procedure is lock-in amplifier discovery or stage delicate discovery [9]. The lock-in amplifier premise is compacting all the signalized data into a restricted transfer speed depends on frequency and enhance transmission capacity [10]. It truly relies upon knowing signal frequency range and stage having slender band signal data. The signals can

be distinguished within the sight of a lot of uncorrelated commotion when the frequency periods of wanted signals are known [11]. Lock-in amplifier is fundamentally a coordinated demodulator followed by a low-pass channel [12]. It intensifies just the part of the information signal at the reference signal recurrence, and channels out any remaining frequencies [13]. Major objective of this research work is to obtain the lesser power dissipation circuit and suitable for various real time application specific circuit. Research contributes to the various researchers by improving the availability of lock in amplifier with various detection and beam forming applications [14]-[18].

The lock-in amplifiers are exorbitant, huge in measurement, substantial and by no means reasonable for versatile instrumentation [19]-[21]. In this manner, coordinated lock-in intensifiers can give a few benefits contrasted with business lock-in amplifier. In this proposed work, the digital lock-in amplifier is designed to reduce the power dissipation by gated clocking technique with analysis of behavioral model. Here the gated clocking in DFF triggers the circuit of lock-in amplifier design [22]-[24]. In this, the power, area and delay is analyzed to get the better performance than existing approach [25]-[26].

Rest of this paper summarized as follows. Section II described the literature survey analysis. Section III presents the proposed working strategy with power optimized logic. Section IV described the experimental results of lock-in amplifier and discusses the performance parameter. Section V concluded the proposed work; finally, the future work applications are described.

Literature survey

Maximiliano O Sonnaillon, et al. (2008) has described the digital lock-in amplifier for random sampling approach with high frequency amplifier. A high-frequency LIA utilizes an arbitrary examining plan is designed and tried tentatively in this review. By utilizing this examining system, it is conceivable to measure, without associating impacts, intermittent signs of frequencies that are a few times higher than the Nyquist recurrence. Insightful and mathematical examinations that show the benefits and constraints of the proposed conspire are introduced. A high-recurrence computerized LIA execution is likewise depicted. The model greatest inspecting recurrence is 150 kHz, and its most extreme sign recurrence without associating is 2.5 MHz, restricted simply by the arbitrary testing time frame quantization [27]-[33].

An Hu, and Vamsy P C, (2010) has presented the CMOS circuit of lock-in amplifier with integrated logic of photo transistors in opto electronic applications. This depict the plan of optoelectronic lock-in amplifier for optical detecting and spectroscopy applications. The model is created utilizing Taiwan Semiconductor Manufacturing Co. CMOS 0.35-μm innovation and utilizations a phototransistor cluster to change over the episode optical signs into electrical flows. The LIA is enhanced to be operational at 20-kHz balance frequency yet is operational in frequency range from 13 kHz to 25 kHz. The framework is tried with a light-emanating diode (LED) as the light source. The commotion and sign contortions are smothered with channels and a stage bolted circle (PLL) executed in the LIA. The yield dc voltage of the LIA is corresponding to the occurrence optical power [34]-[39].

Takashi S and Misato, (2012) has presented the lock-in amplifier. technique is to gauge the attractive hysteresis as an element of temperature. It depends on the otherworldly deterioration of polarization and estimation of various sounds utilizing the symphonious identification capacity of a lock-in enhancer. Applying this technique, an estimating arrangement of the BH circle was planned and manufactured. This framework gives spectra of attractive transition thickness B driven by an air conditioner attractive field h. The BH circles are reproduced from the spectra of the B. The spectra and BH circles were estimated for a NiZn ferrite toroid at different temperatures. At the point when the temperature increments from the room temperature, the higher music of the spectra increment. Moving toward the Curie temperature T C from beneath, attractive misfortune and nonlinearity of the BH circles increment, and the circle shows the immersion just underneath Temperature .

Xiaotao Han, et al. (2012) has proposed the digital lock-in amplifier with magnet based measurement. estimation framework dependent on the Digital Lock-In (DLI) method has been created. A non-inductive reference resistor with high warm soundness is associated with the magnet in arrangement. Two reference signals are created basically. The voltages across the reference resistor and the magnet are utilized as estimation signals which are inspected simultaneously by the Analog-to-Digital Converter (ADC) and prepared with a DLI amplifier performance. The inductance and opposition of the magnet would then be able to be inferred by calculation. The Infinite Impulse Response (IIR) channel plan, estimation framework execution and blunder examination are depicted. The precision of the inductance estimation is superior to 0.01%.

Javier A, et al. (2014) has presented the squae signal based Analog lock-in amplifier for noise reduction. Dual-phase lock-in amplifiers (LIAs) are designed to extract information from signals buried in high noise levels. In spite of their popularity, their use has been traditionally limited to input sinusoidal waves with symmetric power supplies. This paper presents an algorithm that enables single-supply analog LIAs to properly process input square waves. Formed by linear

equations, its computational implementation is much simpler than that of the traditional sinusoidal algorithm. Moreover, applied to battery-operated microcontrolled systems where square signals can be generated by the embedded microcontroller, it presents intrinsic advantages such as simplicity, versatility, and reduction in power and size [40]-[44].

Andrea De M, et al. (2016) has present another completely simple coordinated lock-in amplifier for the precise recognition and the estimation of little, moderate, and uproarious signs, run of the mill of sensors. The LIA incorporated circuit in a 0.35 µm standard CMOS innovation with low-voltage (1.8 V) low-power (2 mW) qualities, plays out a programmed arrangement of the general stage between the information and reference signals, both at power-ON of the framework and for any variety during its working time. Regardless of whether these sorts of amplifier work at a particular single working frequency has been upgraded to work, through a programmed recurrence tuning capacity, in one-decade recurrence variety range, set to [2.5–25 Hz], especially influenced by noise.

Giuseppe C G et al. (2017) has investigated the digital lock-in amplifier with FPGA implementation for adopting brain monitoring applications. Lock-in amplifier generally addresses an incredible strategy making a difference to improve execution in such conditions. In this work a digital LIA framework, in light of a Zynq FPGA has been planned and executed, in an endeavor to investigate. FPGA-based arrangement adaptability has been explored, with specific accentuation applied to computerized channel boundaries, required in the advanced LIA, and its effect on the last signal location and dismissal ability has been assessed. The acknowledged design was a blended between VHDL equipment modules and programming modules, running inside a chip.

Cheng Z, et al. (2020) has presented the FPGA design of digital lock in amplifier circuit with precision of frequency tracking in signal processing. Double stage lock-in amplifiers are intended to extricate data from signals covered in high commotion levels. Regardless of their prominence, their utilization has been customarily restricted to enter sinusoidal waves with symmetric power. The single-supply simple LIAs to appropriately handle input square waves. Shaped by direct conditions, its computational execution is a lot more straightforward than that of the customary sinusoidal calculation. Also, applied to battery-worked microcontrolled frameworks where square signals can be created by the implanted microcontroller, it presents inherent benefits like straightforwardness, flexibility, and decrease in force and size.

Kaushal K and S A Akbar, (2020) has reviewed the LIA for portable sensor applications based interfacings. Here the LIA has been a significant adaptable estimation for extricating low-level signals in noise. Recent past, the significance of LIA has been acknowledged as a sensor interfacing stage and various compact executions focusing on detecting applications have been accounted for. This overviews LIA plan, usage and application as versatile sensor interfaces. The forward short of stage discovers paving the way to the best in class usage in different fields of utilization. Various plans and execution procedures for LIA have been arranged and presented according to the plan geographies. The principle classification being simple, computerized, FPGA and CMOS incorporation.

Proposed method

In this work, the proposed power optimized design of digital lock-in amplifier with ADC incorporations are designed and the power optimization uses the clock gating technique. This is applied on the DFF logic of ADC, LPF triggering states. Lock-in amplifiers are used to detect and measure very small AC signals down to a few nanovolts. Accurate measurements may be made even when the small signal is obscured by noise sources many thousands of times larger. Lock-in amplifiers use a technique known as phase-sensitive detection to single out the component of the signal at a specific reference frequency and phase. Noise signals, at frequencies other than the reference frequency, are rejected and it does not affect the measurement.

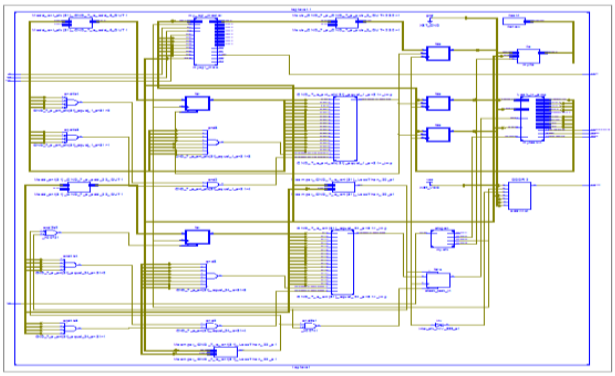

Fig 1. RTL schematic of Lock in amplifier working with ADC

The RTL schematic view of proposed power optimized design of digital lock-in amplifier is shown in figure1. The LIA requires a reference frequency to test the energized and fixed frequency and the lock-in recognizes the reaction from the test at the reference frequency. Lock-in amplifier creates reference signal generally by a stage PLL reference. A LPF with a low frequency decreases the noise. As such, the yield of the channel is a voltage relative to the adequacy of the info signal, while the harmonic is decreased by the coordinated demodulation activity.

The low pass filter eliminates the cut-off frequency components:

$$Cos\,(\,2\omega\,t\,+\,Vr\,+\,Vref\,)\,=\,0 \qquad (1)$$

$$Fs\,=\,fref\,+\,Df \qquad (2)$$

Major performance in digital lock-in amplifier uses the PLL, ADC, LPF and modulator block. The information stage comprises of a pre-enhancer and an addition stage. They pre-measure the input signal covered in commotion by intensifying it to a reasonable level for the demodulator. They likewise increment the sign at the ideal level.

A. Lock-in amplifier with ADC

The increased gain fluctuation of both the DAC and ADC performed on the Lock- in Amplifier. All discrete mixed signal processor in verilog utilizes some timescale to define the time units and goal for the discrete time reproduction. In this model, the module is utilizing the delays inside the framework, thus legitimate activity of the module requires the time unit to be define. The operations of simple LIAs are generally reported. It comprises of the perusing of an mod-signal (Vr), which has a known frequency, and afterward it is multiplied by a reference signal (Vref) of a similar frequency range. This reference might be either a square or a sine structure signal. Accordingly, this multi-measure of another signal (Vrs) of twofold frequency is gotten; and it is balanced by the read signal varieties.

The normal of this resultant signal value is identified with both phase shifting and amplitude variations of input signal.

$$Vr = Ksig\ sin(\omega rt + \theta sig) \qquad (3)$$

$$Vref = Kref\ sin(\omega rt + \theta ref) \qquad (4)$$

$$Vrs = Vr * Vref \qquad (5)$$

For this situation the time unit is 1-nanoseconds, with the goal that delay. Care ought to be taken to pick a timescale and goal for the task so the modules of amplifier determined with binary evaluation in Virtex implementation.

$$Vref(t)\,=\,Vref\ 0\,<\,t\,<\,n\,/\,2 \qquad (6)$$

$$Vref(t)\,=\,-Vref\ T\,/\,2\,<\,t\,<\,n \qquad (7)$$

The entirety of the past models in this part would as it were respond when information changed, so they would work with whatever timescale was fitting for the remainder of the framework.

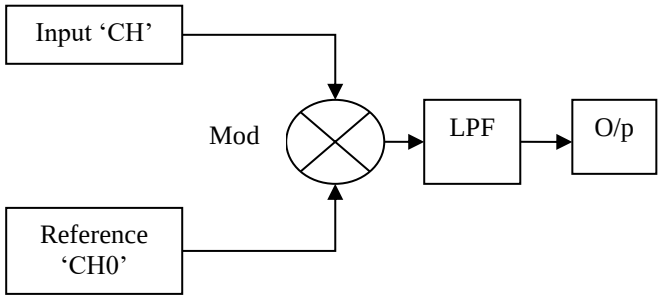

Fig 2. Block diagram of lock-in amplifier

General flow blocking process of lock-in amplifier is shown in figure2. Here it combines operational amplifier and power amplifier performance triggering state. The reference channel gives the duplicated signal; this is generated by PLL and it can be utilized as a source of perspective channel. The demodulator is a full wave rectifier, which amends the information signal by utilizing the reference signal. At the point when the info signal and the reference signal have a same frequency, the demodulator yield has a DC segment corresponding to the information signal abundance and the cosine of the stage contrast between the signals. The change of the period of the reference signal is finished utilizing a reference channel. Consequently, a low-pass channel must be added to the yield of the demodulator. A low-pass channel portrayed by a low profile off frequency is vital to decrease the noise superimposed on the DC signal.

B. Power reduction strategy

Gated clocking strategy for power reduction of VLSI circuit shows the better power optimal design. Here the lock-in amplifier with ADC performance utilized the clock gating technique to improve the performance by reducing the power dissipation. Clock gating in DFF is determined as follows. Here it takes the clock, reset, data and output changed based on the gated clock.

if reset = '0' then
output <= '0';
elsif (clock'event and clock = '1') then

```
if gate = '1' then
output <= data;
end if;
--------------
if reset = '0' then
out <= '0'
elsif (clock'event and clock = '0') then
out <= '0';
elsif (output = '0' and clock = '1') then
out <= '0';
elsif (output = '1' and clock = '0') then
out <= '0';
elsif (output = '1' and clock = '1') then
output <= '1';
end if;
```

Information flags inside the identification transmission capacity set by the LPF consistent and bandwidth yield at a frequency references is given as F = fsig – fref. Input noise with nearby reference frequency 'fref' shows up as commotion at the yield with a data transfer bandwidth of DC to the identification data transfer capacity by bandwidth identity. This mainly focused the measuring very small amplitude AC signals with low frequency performance by varying analysis of frequency.

By preferring frequency reference and input signal, the LPF improves the performance. The design of digital lock-in amplifier is implemented with virtex FPGA on Xilinx ISE and it is digitalized with signal variation as giving binary value to force function of amplifier. This proposed optimal power of digital lock-in amplifier is applicable for various real time applications. The overall performance of lock-in amplifier with power, area and delay analysis is obtained.

Results and discussion

Thus the design of lock-in amplifier with digital performance and power optimal reduction strategy using clock gating in DFF is performed well. The design of amplifier analyses the performance of area, delay and power for getting better implementation results. Here the amplifier logic uses the ADC and modulator circuit. An Analog to Digital Converter is utilized to change over the read signal. Clearly, the changed over goal is identified with the application necessities or the ideal accuracy for the test. To make the convolution cycle, power optimized LIAs utilizes a digital multiplier rather than a simple one as opposed to the simple LIAs. The caught signal is increased each point in turn and passed to a channel module. Advanced multipliers are less expensive than simple multipliers, decreasing the expense of the computerized Lock being developed.

C. Area utilization

Area utilization depends on the slices, Flip Flops, latches, IOB, clocking, etc are the major factor to determine the area analysis of overall VLSI circuit. Table 1 shows the overall device utilization summary.

Table 1: Device utilization summary

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	1,924	54,576	3%
Number of Slice LUTs	6,847	27,288	25%
Number used as logic	6,275	27,288	22%
Number used as Memory	415	6,408	6%
Number of occupied Slices	2,140	6,822	31%
Number of MUXCYs used	6,152	13,644	45%
Number with an unused Flip Flop	5,788	7,599	76%
Number with an unused LUT	752	7,599	9%
No of fully used LUT-FF pairs	1,059	7,599	13%
No. of slice register sites lost to control set restrictions	412	54,576	1%
Number of bonded IOBs	9	218	4%
Number of LOCed IOBs	9	9	100%
Number of RAMB16BWERs	95	116	81%
Number of RAMB8BWERs	1	232	1%
No. of BUFIO2FB/BUFIO2FB_2CLKs	1	32	3%
Number of BUFG/BUFGMUXs	6	16	37%
Number of ILOGIC2/ISERDES2s	2	376	1%
Number of OLOGIC2/OSERDES2s	3	376	1%
Number of BSCANs	1	4	25%
Number of DSP48A1s	8	58	13%
Number of PLL_ADVs	1	4	25%

D. Power utilization

Clocking gating technique is applied to reduce the power dissipation of proposed digital lock-in amplifier. The power analysis of voltage and current flow of circuit improves the analysis of amplifier. The power optimal power reduction strategy is applied on the DFF triggering state of amplifier. XPower analyzer in Xilinx ISE is shown in the figure3.

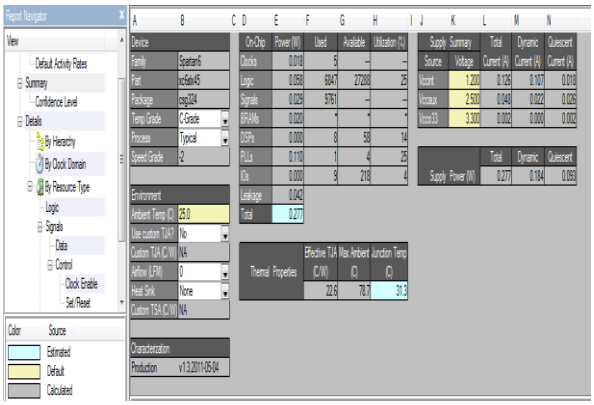

Fig 3. Power report in Xilinx XPower analyzer

E. Delay report

Minimum period: 108.665ns (Maximum Frequency: 9.203MHz)

Minimum input arrival time before clock: 6.690ns
Maximum output required time after clock: 6.098ns
Clock period: 7.745ns (frequency: 129.122MHz)

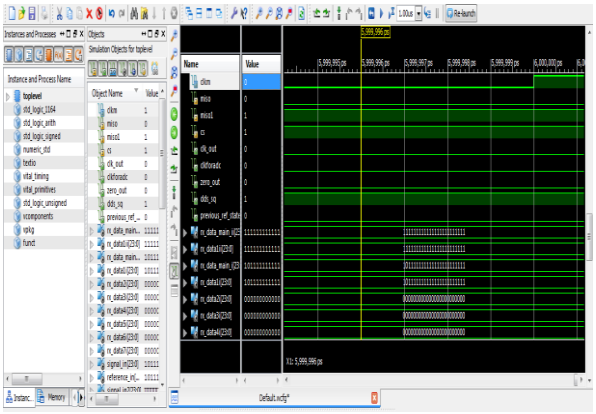

Fig 4. Initial state of amplifier implementation with clock0

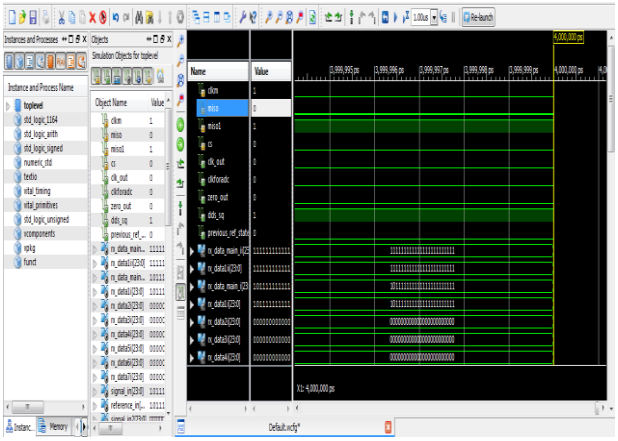

Fig 5. Lock-in amplifier performance of digitalized state

Locks in amplifier variations are taken by digital (binary) values and it uses the major block of PLL, LPF and ADC. Figure 4 and 5 shows the overall analysis of digital lock-in amplifier performances. The analyzed results shows appropriate conduct of lock-in amplifier with ADC implementation and it exhibit relevant to various types of analyses at low frequencies. Because of the sort of power optimal utilized for its turn of

events. Low-frequency application requires identifying adequacy of a regulated signal with least expense and less power utilization. Thus the designing state shows the better variation and optimal power reduction by clock gating is achieved.

Conclusion and future scope

Thus it concluded that, the power optimal lock-in amplifier with ADC logic is designed to obtain the better performance. Here the digitalized logic of lock-in amplifier is used on the various real time applications and it is performed with digital varying logic to get the better performance. Here the analog to digital converter circuit and PLL performed when it gets the logical analysis of clocking strategy to trigger the logic. Specific frequency variation in clocking cycle determines the amplification efficiency. This is applicable to recover the noise state results from given input. This type of VLSI logic determines the removes the half, low frequency and specific sampling frequency signals. Lock-in amplifier performs the detection, demodulation and amplification state of performance for various real time applications. In future, the work may extended with the various comparative analysis of noise reduction strategy and it is designed to applicable for real time application specific design.

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