

Development of Reversible Programmable Gate Array

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ABSTRACT-The model of digital computation used until now is intrinsically irreversible. This is because the two-bit gates used to construct circuits are irreversible as they involve two input bits and only one output bit. Irreversible gates dissipates energy during their operations, in this manner information bits are lost. Reversible Logic is a technique that can lead to circuits run as normal Logic operations, but use less power. In reversible logic the number of inputs and number of outputs must be equal. The input states are reconstructed from output states because of one to one mapping. Using reversible logic gates in the digital circuits it reduces the power consumption and non-destruction of information. In this paper, configurable logic block is designed in reversible manner for Programmable logic array based and multiplexer based field programmable gate array with less number of reversible gates, garbage outputs and quantum cost.

Index Terms: Reversible gate, Garbage output, Quantum cost, Multiplexer

I. INTRODUCTION

Computers now on the market are faster, smaller and more complex than their predecessors. However, the price paid for this speed and complexity is increased power consumption. The primary reasons for the rise in power consumption are the increase in clock frequency and the increased number of

transistors packed onto a chip. In any digital computer, an array of 0s and 1s represents a number. Every operation in a computer corresponds to the manipulation of the bits, e.g., flipping of 0 to 1 or 1 to 0. Some information about the inputs is erased every time a logic operation (function) is performed. Thus, we cannot deduce the inputs from just knowing the outputs alone. In addition, distinct logical states of a computer must be represented by distinct physical states of the computer hardware.

Moore's law describes a long-term trend in the history of computing hardware: the number of transistors that can be placed inexpensively on an integrated circuit doubles approximately every two years. Then the year 2020 or 2030 will find the circuits on an Integrated circuit measured on an atomic scale. We pack more logic elements into smaller volumes and clock them at higher frequencies, more heat will be dissipated. This creates at least three problems: Energy costs money, Portable systems exhaust their batteries and Systems overheat.

When a digital computation system erases a bit of information, it must dissipate $\ln 2 \times kT$ energy [1]. For $T = 300$ Kelvins (room temperature), $k = 2.9 \times 10^{-21}$ joules. Computers now on the market are faster, smaller and more complex than their predecessors. Speed and complexity is increased power consumption. Today's computers erase a bit of information every time they perform a logic operation. These logic operations are therefore called

"irreversible." Information loss is equal to the loss of energy. With the law of physics loss of information is associated requiring that one bit of information lost dissipates $k T \ln 2$ of energy[1].

- where k is Boltzmann' constant
- and T is the absolute temperature of the system.

Irreversible logic is the usage of common gates such as AND, OR, EXOR etc. Irreversible logic circuits dissipate heat for every bit of information lost and irrespective of their implementation technologies. Therefore the input vector cannot be reconstructed from its output vectors in irreversible logic circuits.

II.REVERSIBLE LOGIC

Reversible Logic is a technique that can lead to circuits run as normal Logic operations, but use less power. There should be same number of output lines as the number of input. Two conditions should be following for reversibility in the digital logics [2].

- **The first condition** for any deterministic device to be reversible is that its input and output be uniquely retrievable from each other - then it is called logically reversible.
- **The second condition:** a device can actually run backwards - then it is called physically reversible.

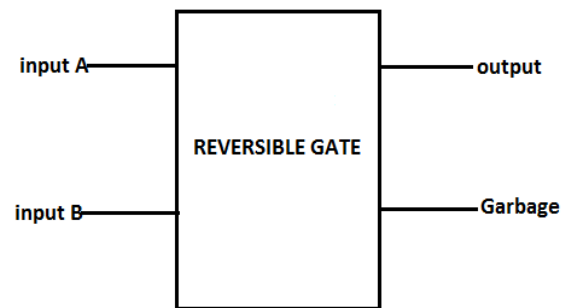
Physical reversibility means towards the retrieval of input by the output. The device follows these two conditions then the second law of thermodynamics guarantees that it dissipates no heat [11]. In the reversible logic fan-out and feedback is not permitted.

III. REVERSIBLE GATE AND PROPERTIES

A Reversible Gate is an-input, n-output (denoted by $n \times n$) circuit that produces a same output pattern for each input pattern

[3]. Reversible Gates are circuits in which the number of outputs is equal to the number of inputs and there is a one to one mapping between the vector of inputs and outputs, i.e., it can generate unique output vector from each input vector and vice versa. A reversible circuit must incorporate reversible gates in it and the number of gates used in a design is always a good complexity measure for the circuit. It is always desirable to realize a circuit with minimum number of gates.

A. Gate Structure and Parameters



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Figure 1. Structure of Reversible gate

a) Garbage Output

Garbage outputs are the unwanted outputs of a reversible circuit. Every gate output that is not used as input to other gate or as a primary output is called garbage. The unutilized outputs from a gate are called "garbage".

b) Number of gates

The total number of gates used in a circuit. Minimum possible number of gates must be used in a circuit.

c) Quantum Cost

This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1×1 or 2×2) required to realize the circuit. The quantum cost of a reversible

circuit is the sum of the quantum cost of its gates.

d) Constant Input

The number of inputs that are kept constant (0 or 1) for synthesis the given functions [3].

IV. REVERSIBLE GATES REVIEW

In the last few years reversible gates like Toffoli gate, Feynman gate, Fredkin gate, Peres gate, New gate has been proposed. Here Feynman gate, Mux gate and Peres gate are reviewed because these gates are used with different configurations[5].

A. MUX Gate

Figure.2 shows the 3×3 reversible gate called MUX (MG) gate. It is a conservative gate having three inputs (A, B, C) and three outputs (P, Q, R). The outputs are $P=A$, $Q=A \text{ XOR } B \text{ XOR } C$ and $R= A'C \text{ XOR } AB$. The Quantum cost of Mux gate is 4.

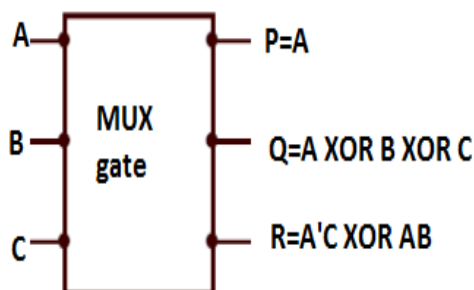


Figure 2. 3×3 MUX gate

B. MUX Gate as AND Gate and OR Gate

In the MUX gate give '0' at the third input C then the output R will get the AND combination of first and second input. Now, the output of the MUX would be "1" only if

the both of the inputs are "1" otherwise it would be "0" for all conditions.

In the MUX gate give '1' at the second input B then the output Q will provide the OR combination of first and third input. Now, the output of the MUX would be "0" only if the both of the inputs are "0" otherwise it would be "1" for all conditions.

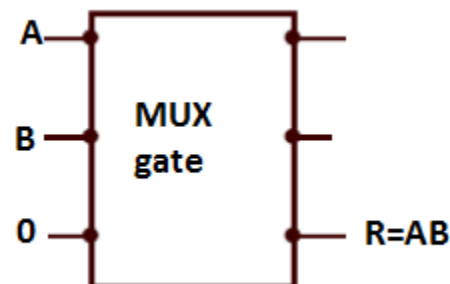


Figure 3. Mux Gate as AND Gate

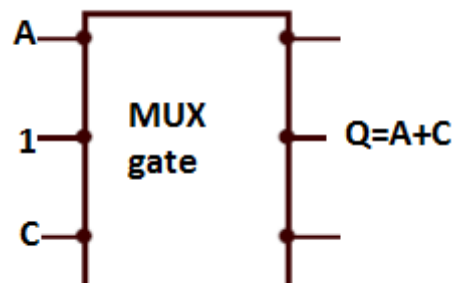


Figure 4. Mux Gate as OR Gate

C. Feynman Gate

An example of a permutation gate is the Feynman gate (called also CNOT gate or Quantum XOR). This gate can be described by the following logic expressions: $(A, B) \Rightarrow (P, Q) = (A, A \oplus B)$. This equation means that the output bit P is just the same as its input A, while on the output of the second wire Q the operation $A \oplus B$ is performed. This operation (EX-OR of A and B) is a standard logic operation. A linear gate is one that all its

outputs are linear functions of input variables. Let a , b , and c be the inputs and P , Q and R the outputs of a gate. Assuming 2×2 Feynman gate, $P = a$, $Q = a \oplus b$, when $a = 0$ then $Q = b$; when $a = 1$ then $Q = \neg b$. Feynman gate is used as a fan-out (or copying) gate. Every linear reversible function can be built by composing only 2×2 Feynman gates and inverters. There exist $8! = 40,320$ 3×3 reversible logic gates, some of them with interesting properties. Figure 5 shows the 2×2 reversible gate called Feynman gate. It has two inputs (A , B) and two outputs (P , Q). The outputs are $P=A$, $Q=A \text{ XOR } B$. This gate can be used to buffer and inverter. The Quantum cost of a Feynman gate is 1 [5].

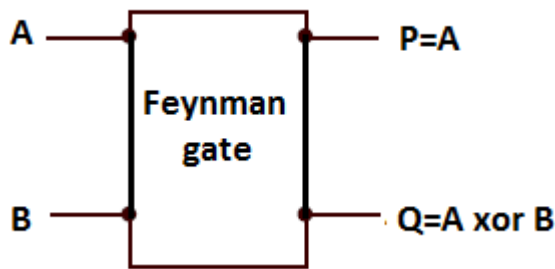


Figure 5. Feynmann gate

D. Feynman Gate as buffer and as inverter gate

The structure of Feynman gate as Buffer & as NOT gate is shown in the figure 6 & 7. If we provide “0” at second input B then gate work as buffer of the given input. If we give “1” at second input the gate work as inverter.

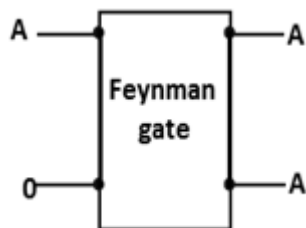


Figure 6. Feynman gate as buffer

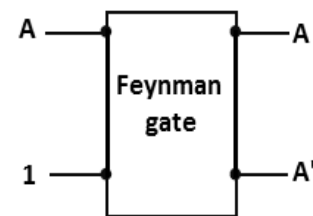


Figure 7. Feynman gate as inverter

E. Peres Gate

Fig 8 shows a 3×3 Peres gate. The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$. The output is defined by $P = A$, $Q = AB$ and $R = AB \oplus C$. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

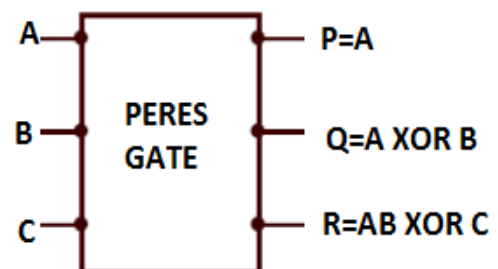


Figure 8. Peres gate

In the Peres gate give ‘0’ at the third input C then the output R will get the AND combination of first and second input. Now, the output would be “1” only if the both of the inputs are “1” otherwise it would be “0” for all conditions.

V. REVERSIBLE LOGIC BLOCK

A. PLA based RLB

A programmable logic array (PLA) is a kind of programmable logic device used to implement combinational logic circuits. The PLA has a set of programmable AND gate planes, which link to a set of programmable OR gate planes, which can then be conditionally complemented

to produce an output. The programmable logic array consists of AND array, OR array, Buffer and Inverter. By using Mux, Peres and Feynman gate with different configurations to construct the reversible logic block. Figure 9 shows the reversible logic block with reversible gates.

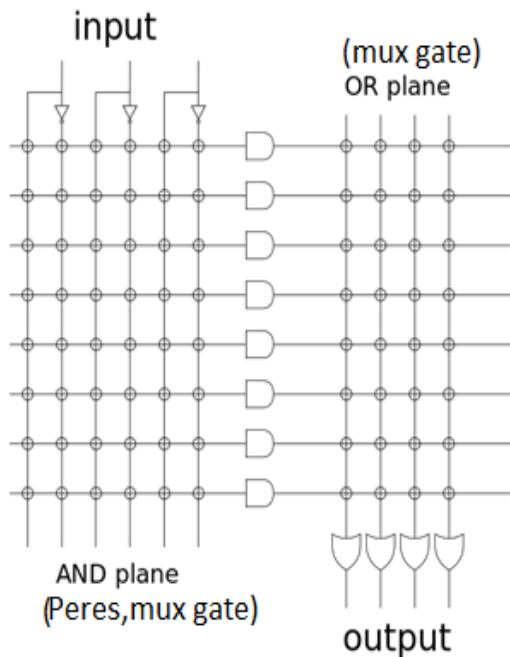


Figure 9. Reversible Array

B. FPGA

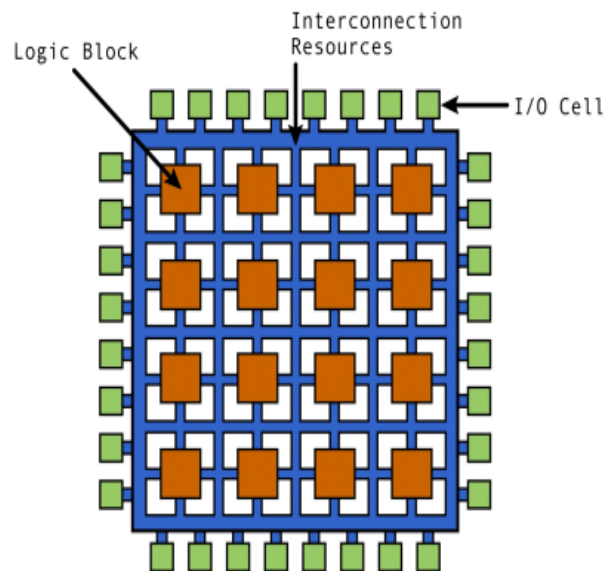


Figure 10. FPGA structure

Field Programmable Gate Array (FPGA) consists of logic blocks, input output cells, interconnection of wires and switches [10]. In the logic block basic building blocks are multiplexer, D-latch. These blocks are developed by reversible gates.

C. MUX based RLB

Multiplexer-based FPGAs utilize a multiplexer to implement different logic function by connecting each input to a constant or a signal. Each block has eight inputs and one output, implementing:

$$f = \left(\overline{s_3 + s_4} \right) \left(\overline{s_1}w + s_1x \right) + \left(s_3 + s_4 \right) \left(\overline{s_2}y + s_2x \right)$$

Multiplexer-based FPGAs can provide a large degree of functionality for a relatively small number of transistors. Multiplexer-based CLBs, however, place high demands on routing resources due to the large number of inputs.

D. 4-to-1 Reversible Multiplexer

A Multiplexer is a device that performs multiplexing. A multiplexer combines more than one input into a single output. In electronics, the multiplexer or mux combines several electrical signals into a single signal. There are different types of multiplexers for analog and digital circuits. For the proposed design of reversible configurable logic block need 4-to-1 reversible MUX. 4-to-1 reversible MUX can be developed using three Mux gates which produces three garbage outputs. The quantum cost of 4-to-1 reversible mux is 12. To design the 8-to-2 reversible MUX we used two 4-to-1 MUXs.

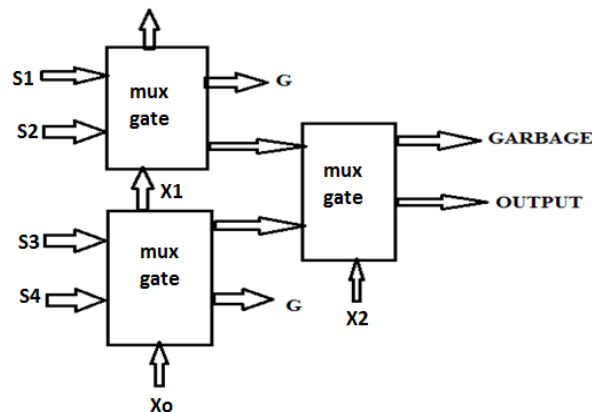


Figure 11.4-to-1 reversible Multiplexer

D. Reversible D-Latch

A D-latch is level triggered. It will follow the input as long as the gate is true. Once the gate goes false, the output will stay at the last known value. Proposed reversible D-Latch with one Mux gate and one Feynman gate. The quantum cost of D-Latch is 5.

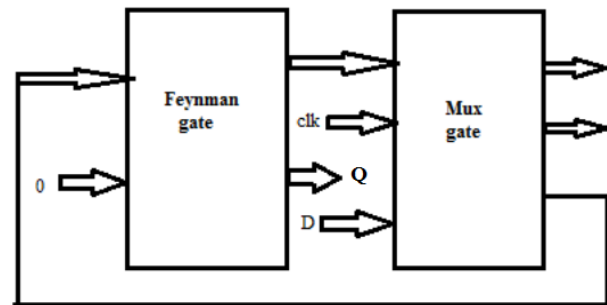


Figure 12. Proposed D-Latch

VI. CONCLUSION

The FPGA technology adopting continues to increase as higher-level tools evolve to deliver the benefits of reprogrammable silicon in the chip manufacturing. In this paper proposed reversible logic block reduces the power consumption. Reversible mux have three gates with quantum cost of 12 and D-latch has the quantum cost of 5. It is less compared to the existing ones. In future all other parts in the FPGA made to be reversible.

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